FRAMATECH

CYCLE : Performance électronique

LES EXIGENCES DE L'IPC A 600

ARIA, Verniolle
Le 26 mars 2025
Sur site

FRAMATECH S.A. au capital de 38112 Euros
Etudes & mises en œuvre de stratégies industrielles internationales Hautes Technologies

4 boulevard d'Arras - 13004 Marseille - France
Tél. +33 491 95 55 70 | Mail : contact@framatech.fr
Organisme de formation n° 93060115506 | Siret 344 351 879 00046 | NAF 742C
Web : www.framatech.fr

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NOTE POUR LE LECTEUR QUI N'AURAIT PAS ASSISTE AU SEMINAIRE :

La documentation ci-jointe est celle qui a servi de support pour illustrer les exposés faits pendant le séminaire **LES EXIGENCES DE L'IPC A 600** et ne représente donc qu'une partie des informations données à cette occasion.

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PLAN DE LA SESSION

Partie A : La fabrication des PCB

Partie B : Les critères d'acceptation essentiels

Partie C: les trouble shooting

Partie D : Documentation accompagnant la livraison (rapports de test/ CofC/ FAI)

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Partie A

La fabrication des PCB

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•Partie A 1: La Fabrication des PCB

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PCB Construction

This training presents PCB basics

- **Vocabulary**
- **Materials**
- **Technologies**

2

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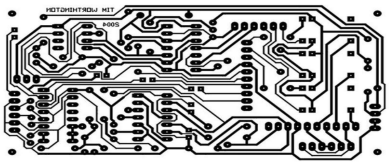
PCB Construction

A Printed Circuit board is simultaneously a :

- Electrical device



PCB Layout

- Mechanical device

- Thermal device

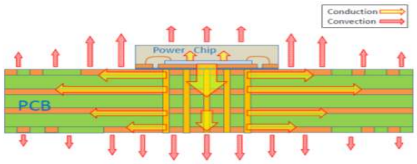


Figure 3. The Heat Flow Directions (Red Arrows)

3

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PCB Construction

PCB Manufacturing challenge !!

- Mechanical ➔ ie :high accuracy for drilling
- Electrical ➔ Dielectric, insulation, high current density, Maxwell skin effect, impedance

Dilectric constant……

- Chemical ➔ µetching, electroless plating, electrolytic plating

(copper, tin, silver, ENIG, ENEPIG…)

4

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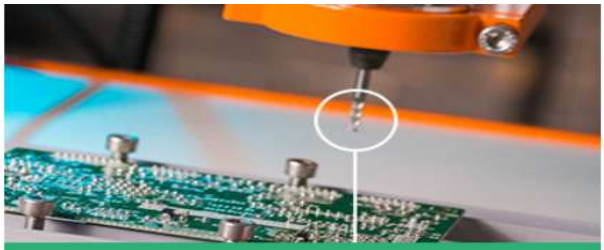
PCB Construction



The holes are drilled to a hairs-width — the drill achieves **100 microns in diameter**, while your hair averages at 150 microns.

5

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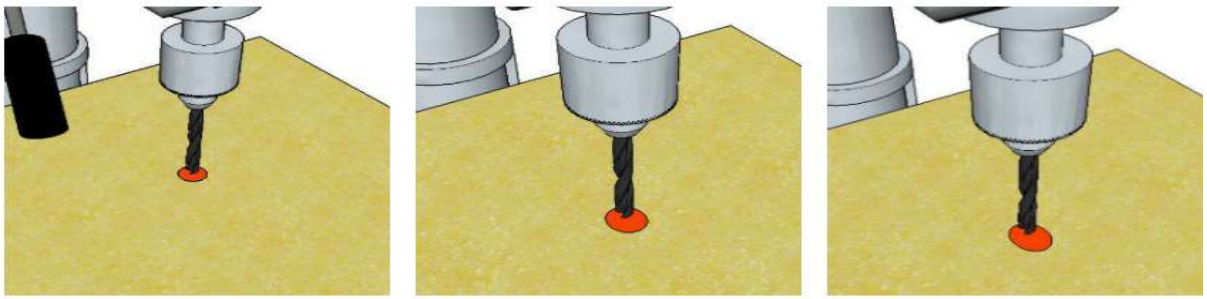
PCB Construction

PCB Manufacturing challenge !!

Run Out



No Run-Out | Slight Runout | Excessive Runout

6

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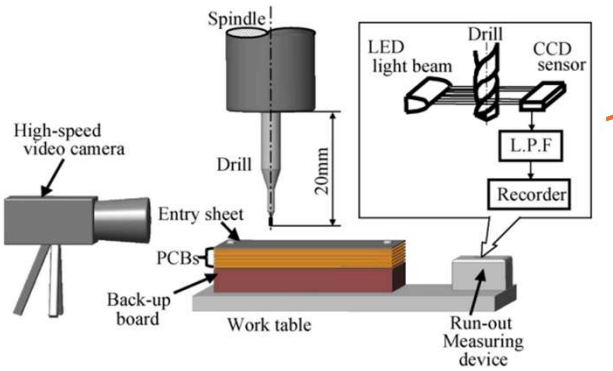
PCB Construction

PCB Manufacturing challenge !!

Mechanical ➔ ie :high accuracy for drilling



Run Out

Drilling

For hole phi : 0,4 mm ➔ TIR< 5 µmm !!

TIR : total indicated run out

Resolution : 1 um !!

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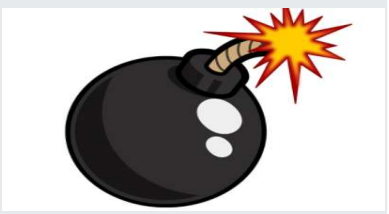
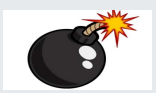
PCB Construction

Key figure

	PCB	The rest
Cost	10 % 	90% 
Issues	70 % 	30% 

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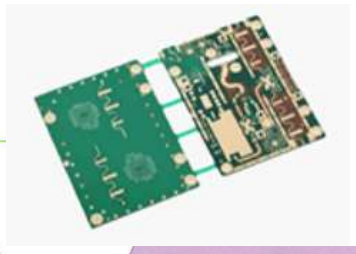
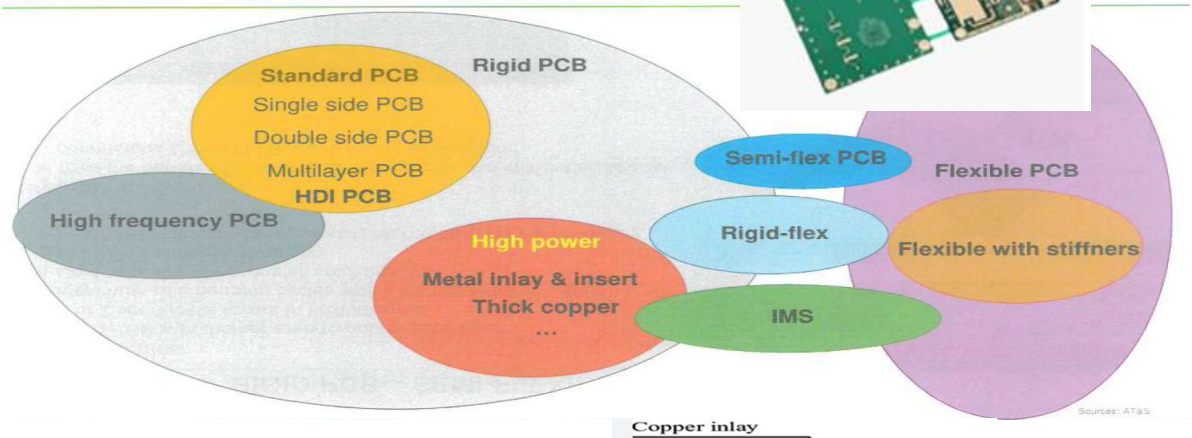
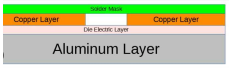
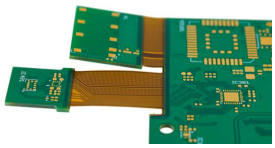
PCB Construction

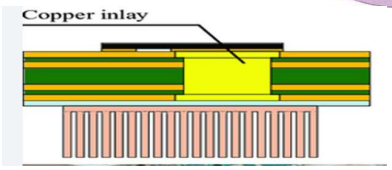


PCB FAMILLY – SUB TECHNOLOGIES









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PCB Construction

Materials

PCB RAW MATERIALS – BASE MATERIALS

Material	Content	Application
CEM1	Epoxy - Paper – Glass cloth	Single & Double side
CEM3	Epoxy – Glass flies – Glass cloth	Single & Double side
FR4	Epoxy – Glass cloth (Flame Retardant 4)	Single, double, Multilayer
PI	Polyimide	Flex & Rigid flex
LCP	Liquid Cristal Polymer	Flex & Rigid flex
PPE	Polyphenylenether	High frequency
HF	Hydrocarbon / ceramics	High frequency
PTFE	Polytetrafluoreten (Teflon)	High frequency
BT	Bismaleimide-triazine-epoxies	Specific applications
CE	Cyanat-ester	Specific applications
Others...		

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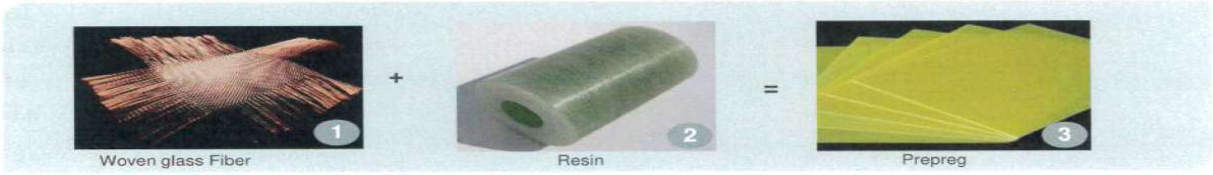
PCB Construction

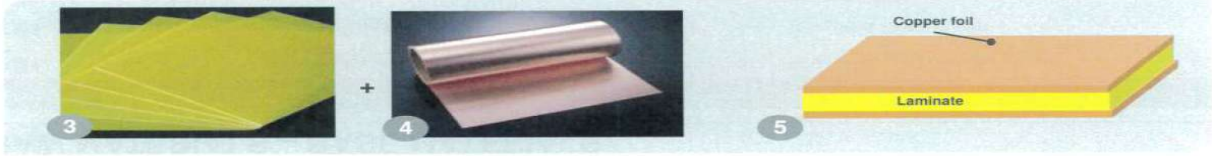
Materials

FR4

▶ 1 Fiber + 2 resin = 3 **Prepreg** (or pre-impregnated)



▶ 3 Prepreg + 4 Copper clad laminate (CCL)= 5 **Laminates (CORE)**



Note: Prepregs and laminates are classified in norms IPC 4101 / MIL-P-13949

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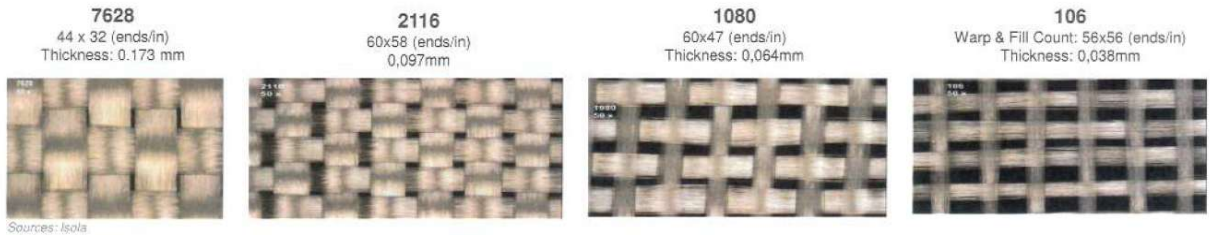
PCB Construction

Materials

IPC 4412 : Specification for Finished Fabric Woven from "E'' Glass for Printed Boards

Examples of woven glass fibers style



Glass fiber style shall be defined by customer, for dielectric specificities and DFM/Reliability
For instance, Thick fiber (7628) are not recommended for Small Size Hole (< 800 um)

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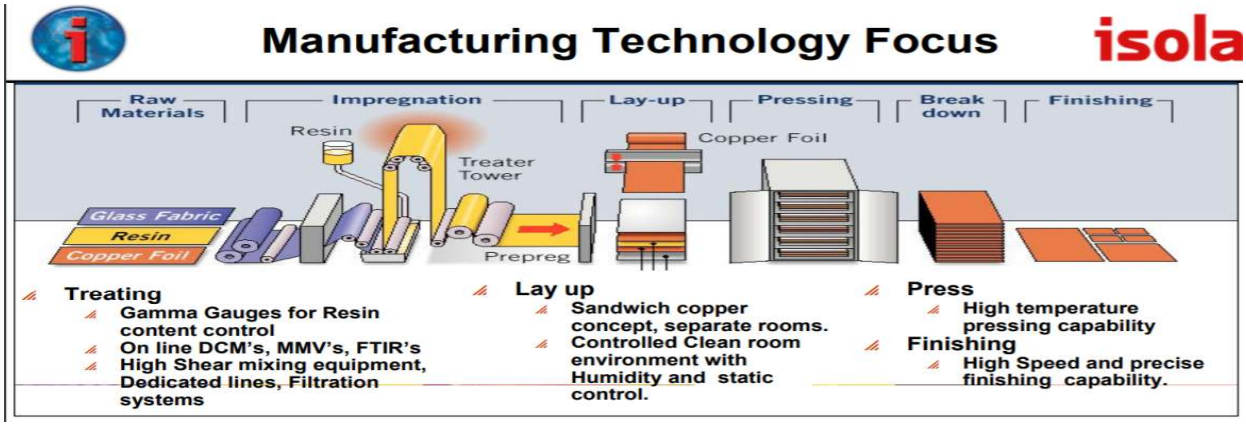
PCB Construction

Core construction



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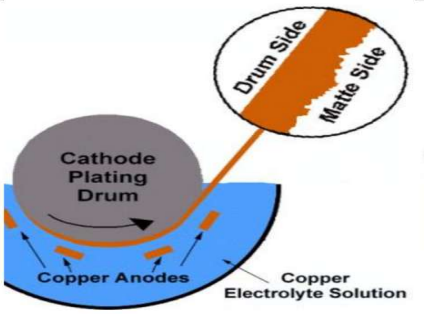
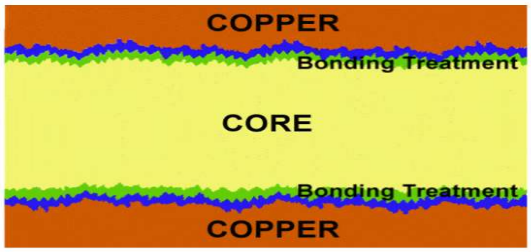
PCB Construction

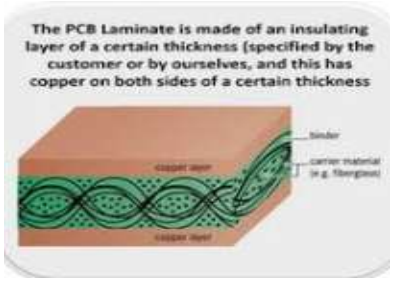
Core construction

Copper foil µetch for **tooth profile**



Standard Foil Clad Laminate





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PCB Construction

Double side

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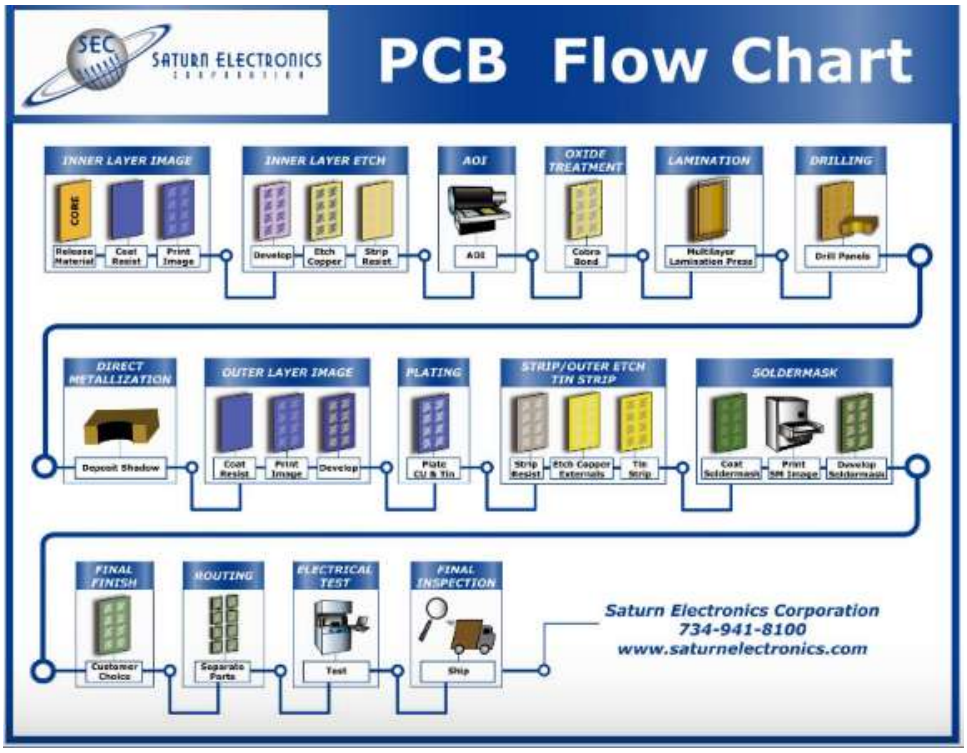

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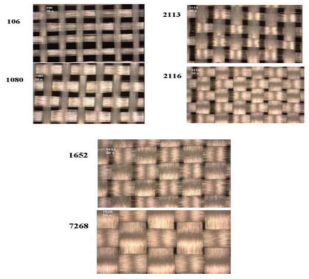
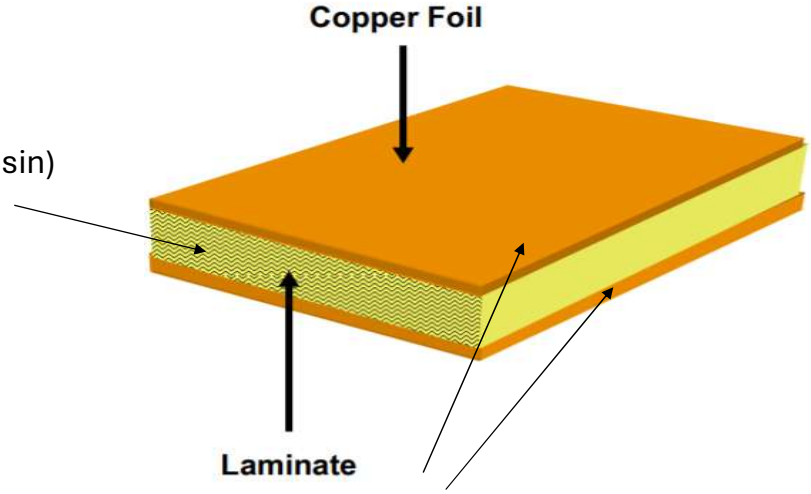
PCB Construction

Double side

Core (woven glass+ epoxy resin)





Copper clad (8/17/34/68 µm)

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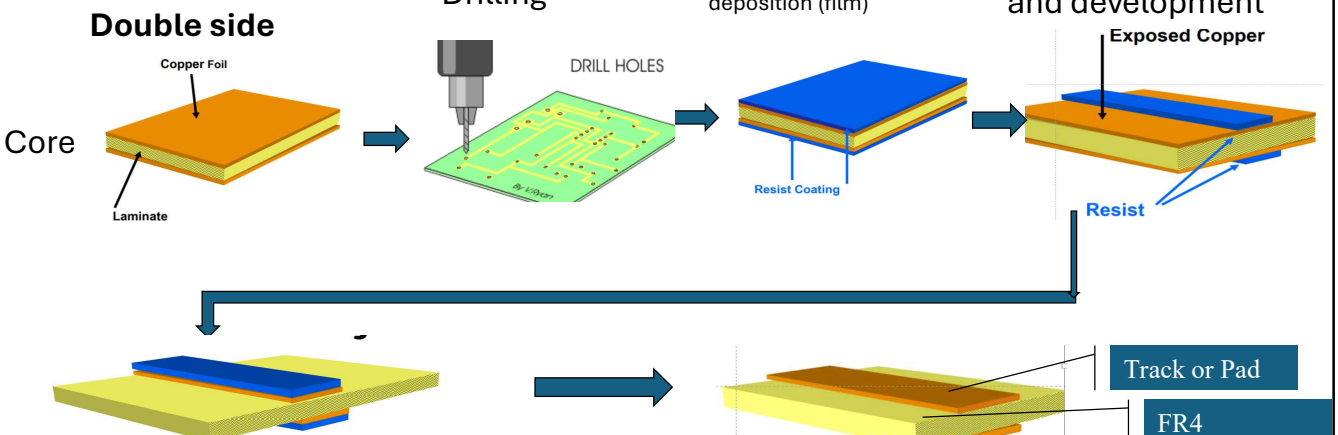
PCB Construction

Double side

Drilling

Photo resist deposition (film)

UV light exposure and development



Copper etching (amoniaca)

Photoresist presence prevents copper from etching

Photoresist stripping

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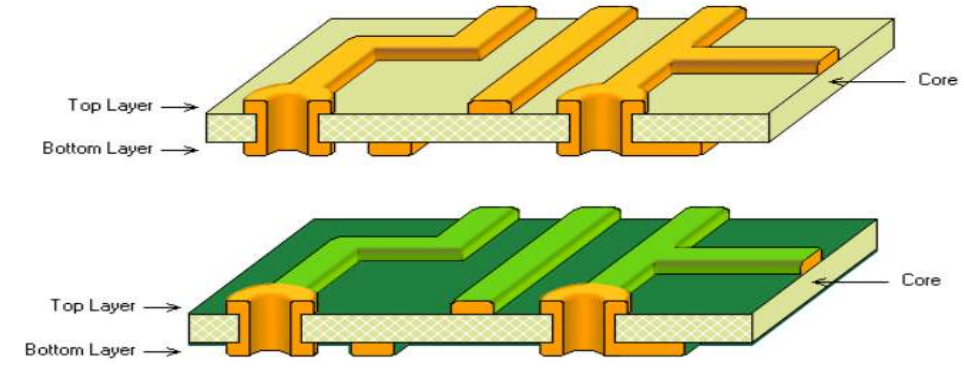
PCB Construction



A double-sided PCB with plated through holes and solder mask.

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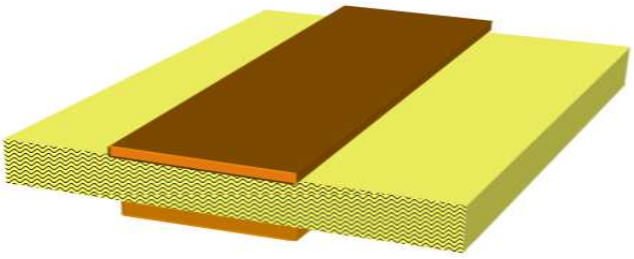
PCB Construction

Multilayer



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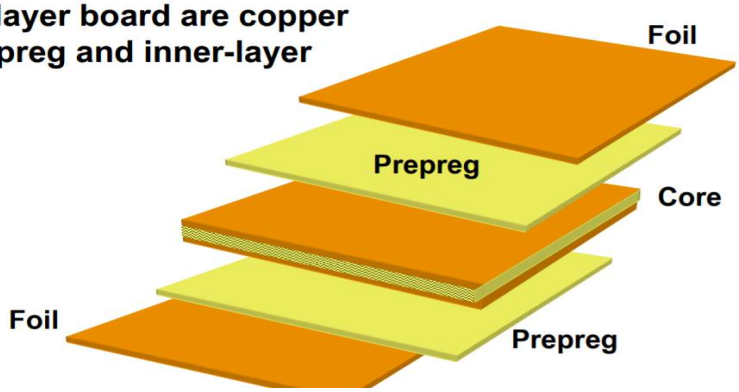
PCB Construction

Multilayer

The basic materials needed to build a multi-layer board are copper foil, prepreg and inner-layer cores.



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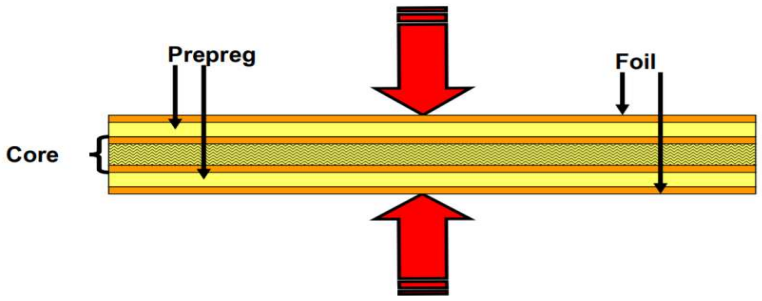
PCB Construction

Multilayer

Inner layer core, copper foil and prepreg are bonded together under heat and pressure, sometimes in a vacuum, during the lamination process. The result is a panel with several layers of copper inside as well as the foil on the outside.



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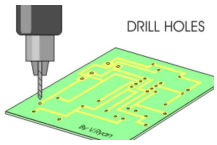
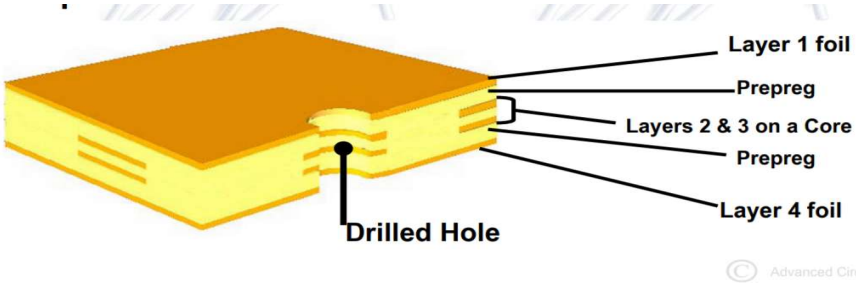
PCB Construction

Multilayer

Drilling





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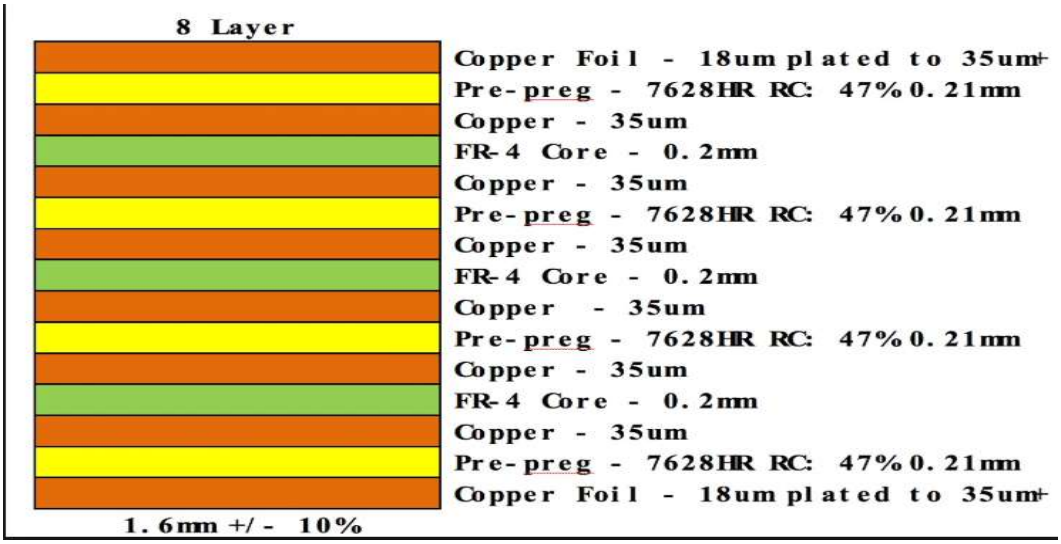
PCB Construction

Multilayer Stack up



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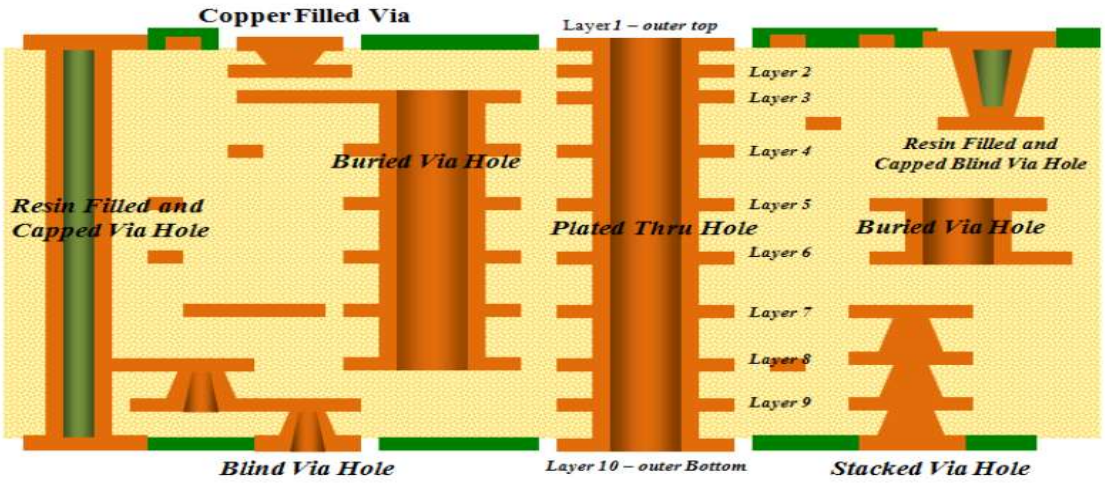
PCB Construction

Construction of a multilayer PCB



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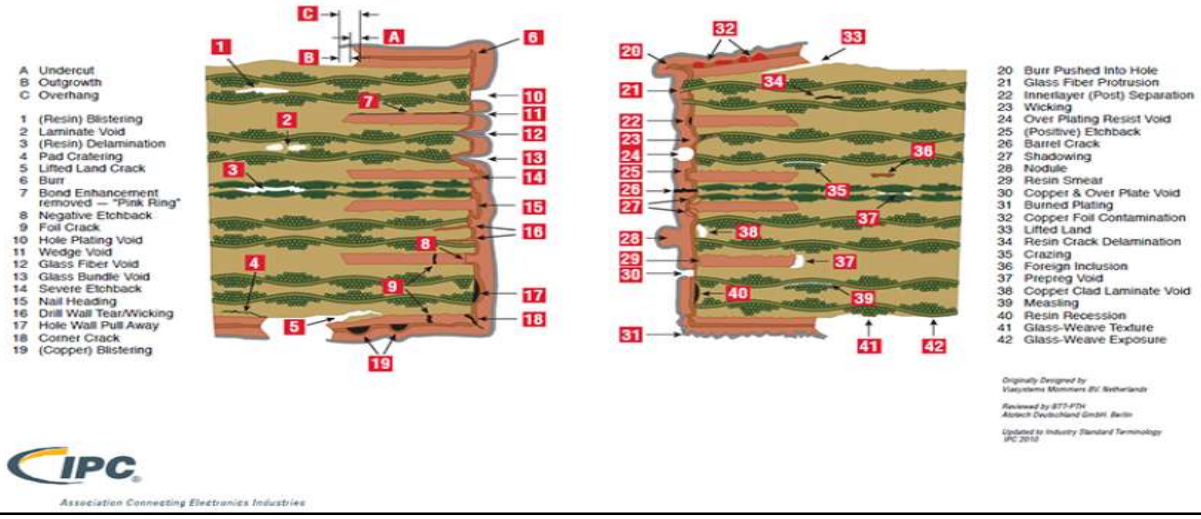
PCB Construction

Plated Through Hole Manufacture

Phenomena in Cross Section of Plated Through Holes



IPC
Association Connecting Electronics Industries

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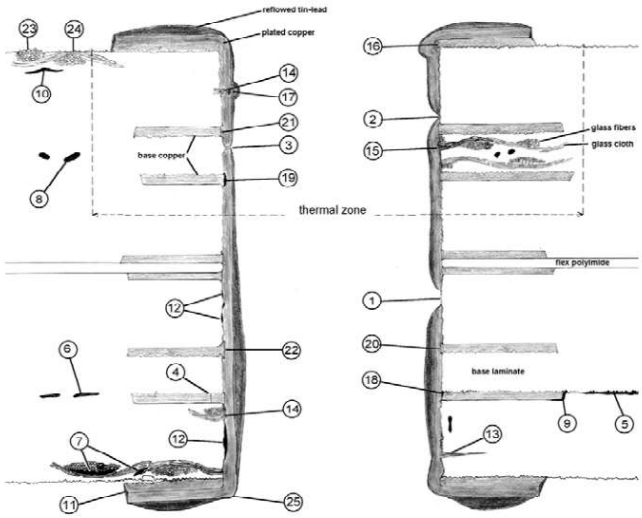
PCB Construction



Cross section of a flex-rigid multilayer plated-through hole with typical features and defects

Example of plated-through hole microsection

1 - plating void
2 - pinhole
3 - plating crack
4 - basic copper crack
5 - delamination
6 - delamination
7 - measling
8 - laminate void (out of thermal zone)
9 - resin recession innerlayer
10 - resin crack
11 - lifted land
12 – pull away
13 - wicking (copper)

14 - glass fibre protrusion
15 - rough drilling and wicking (copper)
16 - burr
17 - plating nodule
18 - smearing
19 - adhesion defect
20 - positive etch back (inner layer copper imbedded in plated copper)

21 - negative etch back
22 - nailheading
23 - weave exposure (fibres visible)
24 - weave texture (glass cloth shape visible)
25 - tin lead thickness < 1µ in angles

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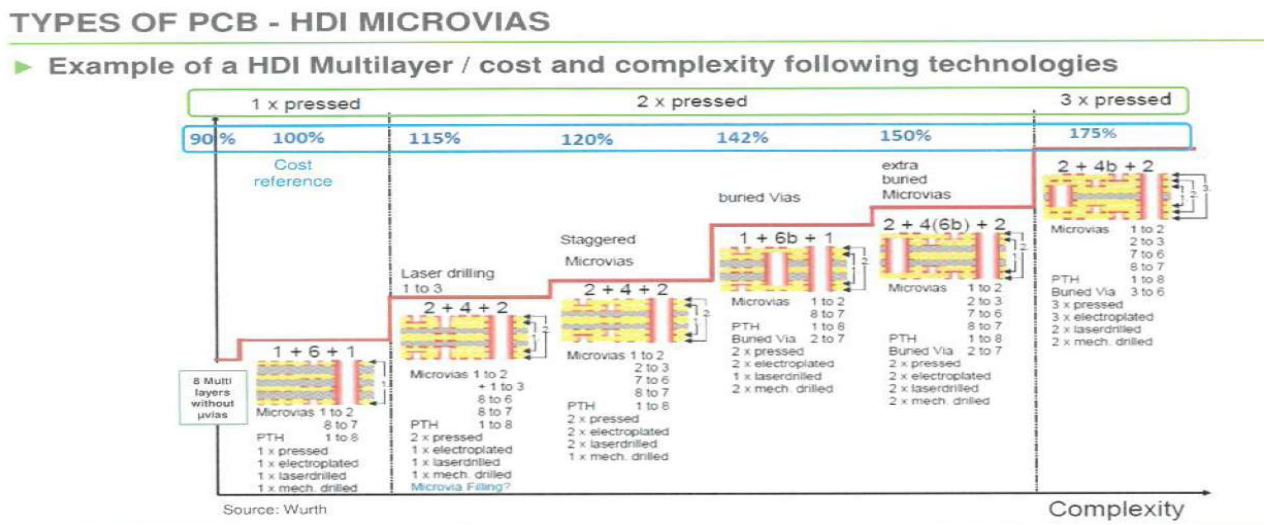
PCB Construction



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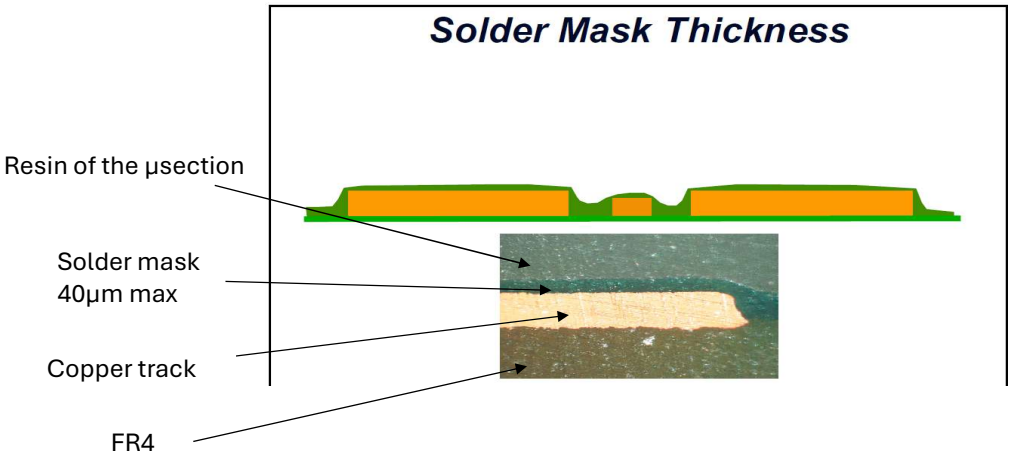
PCB Construction

Solder Mask



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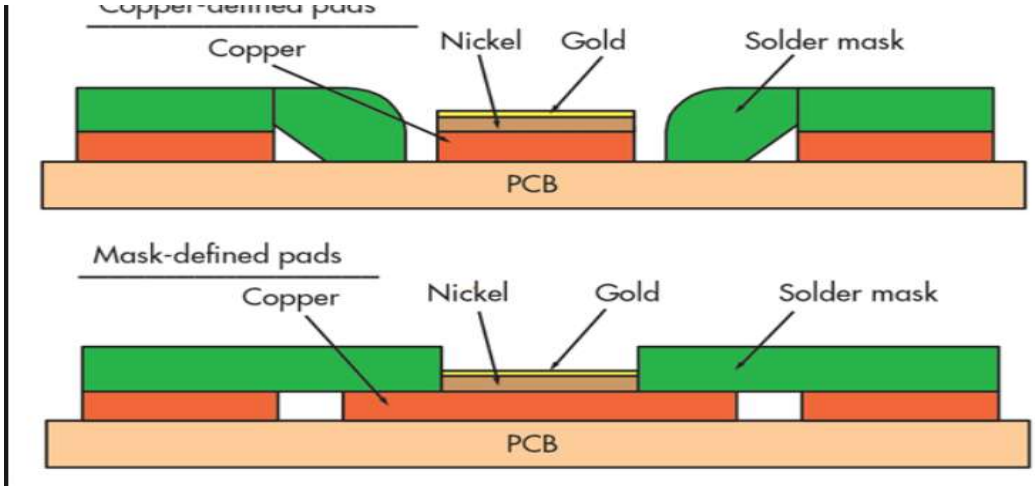
PCB Construction

Solder Mask

NSMD : Non Solder Mask Define



SMD : Solder Mask Define

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PCB Construction

Selective metal finish

- HAL : (dipping in bath SnPb 60/40 , SAC)
- Chemical Tin : Tin whiskers risk
- Chemical silver : short time preservation
- OSP : cannot afford 2 reflows

ENiG : electroless Nickel Immersion Gold
Ni : 5 µm
Au : 100 nm

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PCB Construction

Selective metal finish matrix

	HASL	OSP	Imm Silver	Imm Tin	ENIG	ENEPIG
Planarity	No	Yes	Yes	Yes	Yes	Yes
Solderjoint	Cu-Sn	Cu-Sn	Cu-Sn	Cu-Sn	Ni-Sn	Ni-Sn
Relative Cost	$	$	$$	$$	$$$	$$$
IPC Shelf Life	No Specification	No Specification	12 months	12 months	12 months	12 months
Reflows	6	4	6	2	6	6
Contact	E-Test, ICT	Difficult	E-Test, ICT, Keypad	E-Test	E-Test, ICT, Keypad	E-Test, ICT, Keypad
Press Fit	Good	Good	Good	Good	Good	Good
Au Wirebond	No	No	No	No	No	Yes
Al Wirebond	No	No	Yes	No	Yes	Yes

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PCB Construction

https://www.allaboutcircuits.com/technical-articles/which-via-should-i-choose-a-guide-to-vias-in-pcb-design/

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PCB Construction

Review of a PCB CofC supplied by XXX
(XXX, PO 7053105 , PN 1007-131-01-C3 , DC1832)

Tous les item sont passés en revue, expliquées (avec conversion des unités)
Un conversisseur nous aide à passer des unités anglo saxonnes à métrique avec leur multiple et sous multiples

SHANGHAI UNITECH ELECTRONICS CO.,LTD.
INSPECTION REPORT

CUSTOMER: ACTIA SA
BOARD SIZE: 8.3070"×7.4180"

PART NO.: 1007-131-01 C3
SERIAL NO A95Z020

ITEM	DESCRIPTION		TEST METHOD	NO. OF SAMPLE	SPEC	RESULTS	REMARKS
1	LAMINATE MATERIAL		NA	NA	FR-4	FR-4	
2	BOARD THICKNESS		IPC-6012C 3.4	5 ARRAY	0.0647"±0.0064"	0.0637 "	
3	FLAMMABILITY CLASS		IPC-6012C 3.2.1	NA	94V-0	94V-0	
4	CONDUCTOR WIDTH		IPC-6012C 3.5.1	5 ARRAY	0.00360"~0.00492"	0.0048 "	
5	CONDUCTOR SPACE		IPC-6012C 3.5.2	5 ARRAY	0.00320"~0.00480"	0.0040 "	
6	ANNULAR RING		IPC-6012C 3.4.2	5 ARRAY	MIN. 0.0020"	0.0040 "	
7	CORE	THICKNESS OF CORE	IPC-6012C 3.6.2	NA	0.008"±0.001" 0.015"±0.0015"	0.00787 " 0.01468 "	

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PCB Construction

Review of a PCB CofC supplied by XXX (cont'd)
(XXX , PO 7053105 , PN 1007-131-01-C3 , DC1832)

7	CORE	THICKNESS OF CORE	IPC-6012C 3.6.2	NA	0.015"±0.0015"	0.01468 "	
		COPPER FOIL	IPC-6012C 3.6.2	NA	follow stack up 1/1oz	1/1oz	
8	COPPER THICKNESS	PTH	IPC-6012C 3.6.2.11	1 ARRAY	MIN. 0.0007"	0.00110 "	
		BVH			NA	NA	
		IVH			NA	NA	
		Vias filling	IPC-6012C 3.6.2.16	1 ARRAY	NA	NA	
9	S · M · MATERIAL / COLOR		IPC-6012C 3.7	NA	L.F. / GREEN	OK	
10	LEGEND MATERIAL / COLOR		IPC-6012C 3.2.10	NA	NA	NA	
11	THERMAL STRESS TEST	SURFACE	IPC-TM-650 2.6.8	1 ARRAY	288±5 C 10 SECS	OK	
		PTH			288±5 C 10 SECS	OK	
12	SOLDERABILITY TEST		ANSI/J-STD-003 test C	1 ARRAY	MIN 95%	OK	
13	ELECTRIC TEST		IPC-TM-650 2.5	ALL	≧250V ≦25Ω ≧30MΩ	OK	
14	Adhesion	Finich	IPC-6012C 3.7.2	1 ARRAY	NO PEELING	OK	
		Soider resist			NO PEELING	OK	

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PCB Construction

Review of a PCB CofC supplied by Unitech (cont'd)
(Unitech, PO 7053105 , PN 1007-131-01-C3 , DC1832)

ITEM	DESCRIPTION		TEST METHOD	NO. OF SAMPLE	SPEC	RESULTS	REMARKS
15	TAPE TEST OF LEGEND		IPC-TM-650 2.4.1.1	1 ARRAY	NA	NA	
16	TAPE TEST OF GOLD FINGER		IPC-TM-650 2.4.1	1 ARRAY	NO PEELING	OK	
17	TAPE TEST OF SOLDER MASK		IPC-TM-650 2.4.28.1	1 ARRAY	NO PEELING	OK	
18	WARP & TWIST		IPC-TM-650 2.4.22	5 ARRAY	MAX . 0. 7%	OK	
19	SOLDER THICKNESS		IPC-6012C 3.2.7	5 ARRAY	NA	NA	
20	SOLDER MASK THICKNESS		IPC-6012C 3.7.3	5 ARRAY	0.0004"~0.0012"	0.00082 "	
21	GOLD THICKNESS		IPC-6012C 3.2.7	5 ARRAY	MIN. 1.9685μ"	2.79 μ"	
22	NICKEL THICKNESS		IPC-6012C 3.2.7	5 ARRAY	118.11-236.22μ"	221.6 μ"	
23	INOIC CONTAMINATION	BEFORE SM	BELLCORE GR-78-CORE 14.5	1 PNL	≦3.2ug NaCl / sq.in	0.37ugNaCl / sq.in	
		AFTER FINISH		1 ARRAY	≦3.2ug NaCl / sq.in	0.00ugNaCl / sq.in	

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PCB Construction

PCB technical Definition

Board fabrication and quality acceptance per IPC-6012 Class II and IPC-A-600 class II
These detailed notes and instructions may supersede IPC requirements

Design Information			
Board technology	Outers min trace/space	0.10 mm	
	Outers min annular ring	0.55	
	Inners min trace/space	0.10 mm	
	Inners min annular ring	0.55	
	Min Via drilled diameter / pad diameter	0.25/0.45 mm	
Circuit type / N° of layer	8		
Product performance classification	Class 2	PCB Producibility level	Level C
Material			
FR4	Specification sheet IPC-4101B/99		
Lead free requirements		Material thermal properties minimum values	
	Tg	> 170 °C	
	CTE_z Pre/Post Tg	< 60 /300 ppm/°C	
	Td	> 330 °C	
	T_{260}/T_{288}	> 30/5 minutes	
Board Thickness / Tolerance	1.58 +/- 10% mm excluding solder mask		
Base Copper thickness	See PCB Stack-up		
Outer Finished thickness	35 µm min		
PTH minimum copper thickness	25 µm min		
Plated hole tolerance :	+/-3MIL		
Non-plated hole tolerance:	+/-2MIL		
PTH and NPTH slot tolerance :	+/-5MIL		
Track finish			
ENIG (IPC-4552)			
Board finish			
Solder Mask	LPI	IPC-SM-840	
Colour	Green		
Legend / colour	No		

Impedance Matching

Layer	Trace width (mil)	Trace width (mm)	Impedance (Ohm)	Tolerance	(S)ingle ended / (D)ifferential	Differential distance (mm)	Comment
1		0.850	50	+/- 10%	S	-	RF (ref layer 3)
		0.650	50	+/- 10%	S	-	RF (ref layer 3)
		0.100	100	+/- 10%	D	0.180	Ethernet, FlexRay, CAN
		0.191	40	+/- 12.5%	S	-	DDR
		0.120	90	+/- 10%	D	0.170	USB
		0.132	50	+/- 10%	S	-	HSIC
3		0.120	50	+/- 10%	S	-	RF (GPS 1575MHz)
6		0.128	80	+/- 10%	D	0.101	DDR
		0.120	90	+/- 10%	D	0.149	USB
8		0.191	40	+/- 12.5%	S	-	DDR

Stack-up and/or trace widths may be adjusted to obtain specified impedance matching.

Additional requirement

Plugged vias	Yes, IPC-4761 type VI b	- Except via holes open on both sides (these shall not be plugged)
V-cut specification	(0.6+/-0.127mm)*(30°+/-5°)	
Electrical test	According to IPC-9252	- Net list testing - Simultaneous double side testing
Approval	UL approval according to 94-V0	
Marking	- Manufacturer's logo / date code in solder mask (Id Fab area) - PCB RoHS markings must comply with IPC-1066. The preferred location for the marking is on the printed circuit board top layer. The method, e.g. screen print, etch, label etc. for marking of the printed circuit board is optional but shall be legible to corrected, unmagnified vision	

Pb

PCB STACK-UP

LPI	µm	Solder Mask	MaskTop	A	-	gts
(*)18	µm	Cu Foil	Layer1	1	-	gtl
76	µm	Prepreg				
35	µm	Cu	Layer2	2	-	g1
380	µm	Core				
35	µm	Cu	Layer3	3	-	g2
100	µm	Prepreg				
35	µm	Cu	Layer4	4	-	g3
200	µm	Core				
35	µm	Cu	Layer5	5	-	g4
100	µm	Prepreg				
35	µm	Cu	Layer6	6	-	g5
380	µm	Core				
35	µm	CU	Layer7	7	-	g6
76	µm	Prepreg				
(*)18	µm	Cu Foil	Layer8	8	-	gbl
LPI	µm	Solder Mask	MaskBot	9	-	gbs

* Copper thickness is starting base thickness and does not include plating

Related documents

PCB manufacturing data	1007-111-01_Panel PCB mfg data (Gerber)_C3.zip Note: Use 1007-131-01_Panel PCB mfg data (Gerber)_C3.zip for production (includes 2 boards on one panel)

09	TG	Released for C3 board	2016-05-27	
08	SJ	Added 650µ 50ohm trace and changed L3 RF to 120µ. Changed tolerances (updated for A3 board)	2016-02-29	
07	TG	Released for C2 board (no formal changes)	2015-10-28	
06	TG	Updated for C1 board based on comments from B3 manufacturing	2015-07-12	
05	TG	Updated for C1 board based on comments from B3 manufacturing	2015-07-10	
04	MJ	Updated for B3 board based on comments from B2 manufacturing	2015-06-22	
03	MJ	Updated for B2 board based on comments from B1 manufacturing	2015-05-13	
02	PP	Added 50 (0.132mm) geometry, DDR clock on layer 6 instead of 3	2014-07-07	
01	RJ	Changed impedance matching for RF on layer 1	2014-02-12	
Ind.	Resp.	Nature of change	Date	Appr.

NE-583 30 Linköping, Sweden

Material / Heat treatment / Surface treated

Printed Circuit Board Specification

Lead Free

Document Number: **1007-111-01 C3**

Index: - 09

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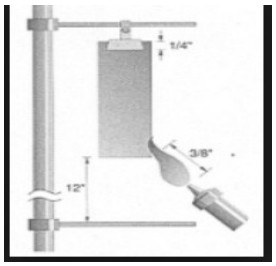
PCB construction

UL System



Classifications [edit]

From lowest (Least flame-retardant) to highest (Most flame-retardant):

- **HB**: slow burning on a horizontal specimen; burning rate < 76 mm/min for thickness < 3 mm or burning stops before 100 mm
- **V-2**: burning stops within 30 seconds on a vertical specimen; drips of flaming particles are allowed.
- **V-1**: burning stops within 30 seconds on a vertical specimen; drips of particles allowed as long as they are not inflamed.
- **V-0**: burning stops within 10 seconds on a vertical specimen; drips of particles allowed as long as they are not inflamed.
- **5VB**: burning stops within 60 seconds on a vertical specimen; no drips allowed; plaque specimens may develop a hole.
- **5VA**: burning stops within 60 seconds on a vertical specimen; no drips allowed; plaque specimens may not develop a hole.

Faire une recherche sur le site UL (https://iq.ulprospector.com/fr/) (E333416 CSI)

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PCB construction

- **Troubleshooting for PCB fabrication process ➔ See IPC 9121**

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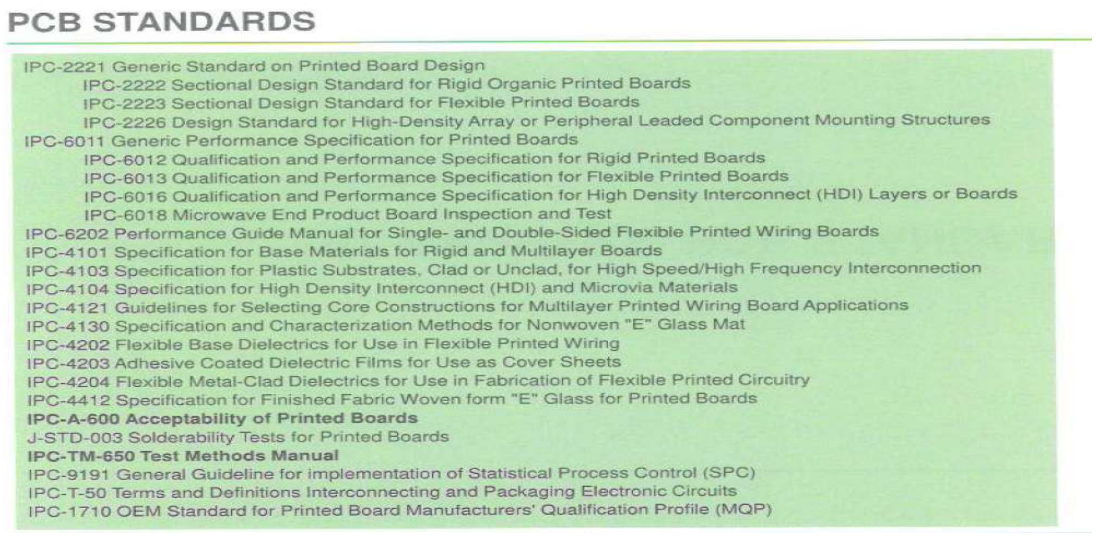
PCB Construction

- IPC IPC IPC IPC IPC IPC IPC IPC IPC IPC IPC



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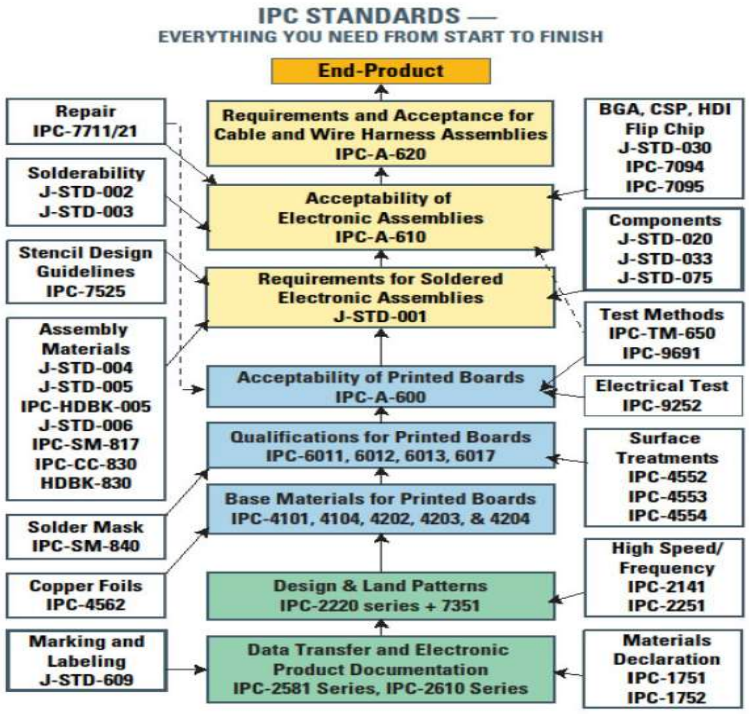
PCB Construction

- IPC IPC IPC IPC IPC IPC IPC IPC IPC IPC IPC



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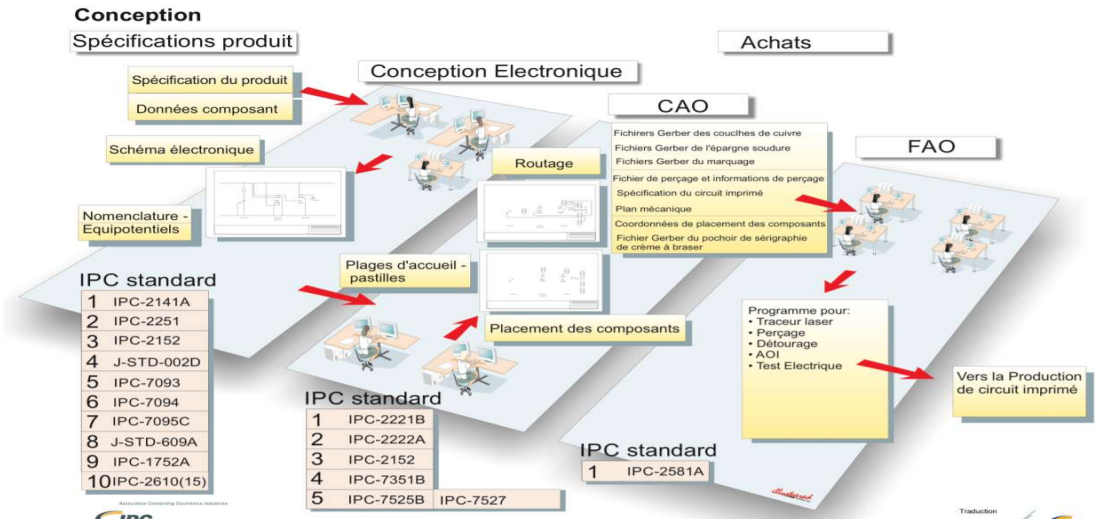
PCB Construction



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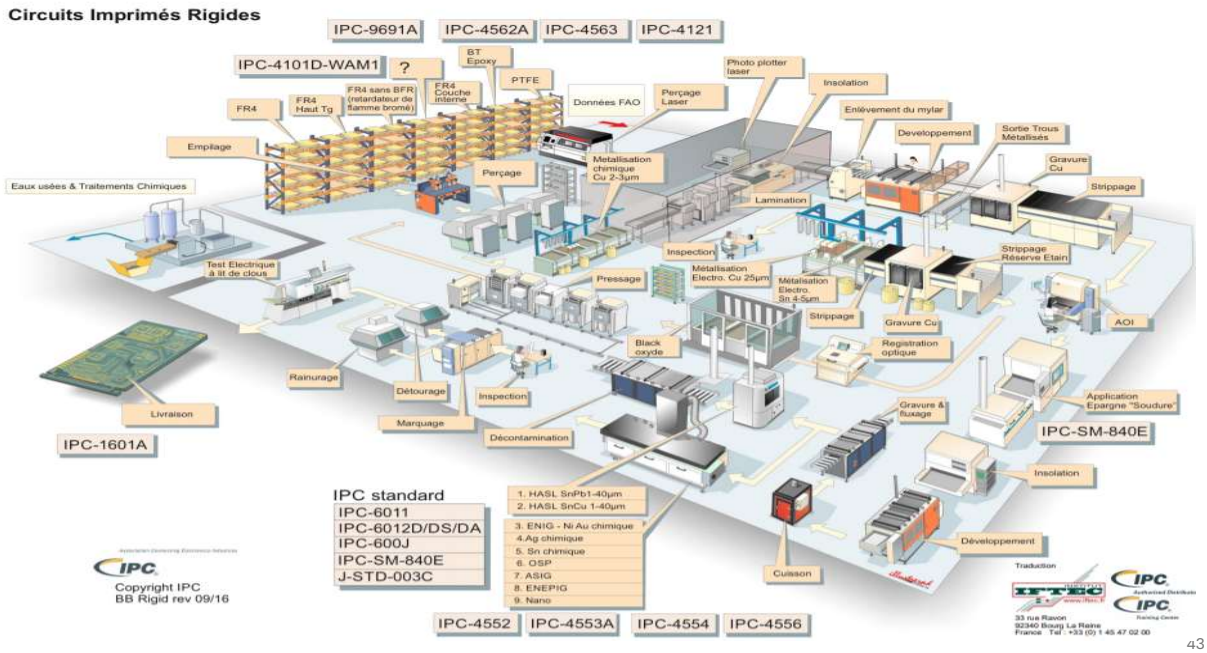
PCB Construction



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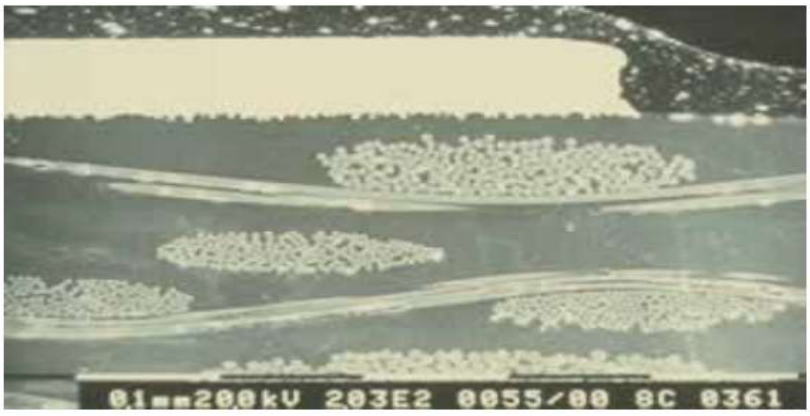
PCB Construction



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PARTIE A-2 SURFACE FINISH

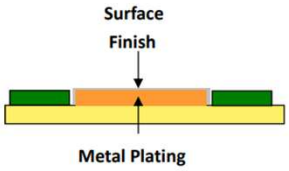
R.M.E.

1

Surface Finish
Fonction et structures génériques

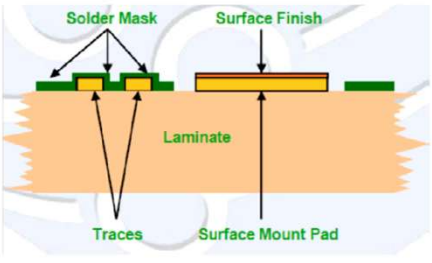
A surface finish may be defined as a "coating"

- located at the outermost layer of a PCB
- (which is dissolved into the solder paste upon reflow or wave soldering)



Two Main Types of Coatings

- Metallic
- Organic



Note:

- (Base) Metal Plating is typically copper (in most cases).
- But, in a few (like ENiG) the Nickel-phosphorous

R.M.E.

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Surface Finish Selection Approach

- *Component Procurement:* Select the cheapest one and let the engineers figure out how to use it.
- *PCB Engineer:* Select the finish that is easiest for the suppliers to provide (their sweet spot); let the assembler figure out how to use it.
- *Assembly Engineer:* Select the finish that provides the largest process window for assembly and test.
- *Sustaining Engineer:* Select the finish that minimizes field failures.
- *CEO:* Select the finish that minimizes the overall cost (including reliability risk).

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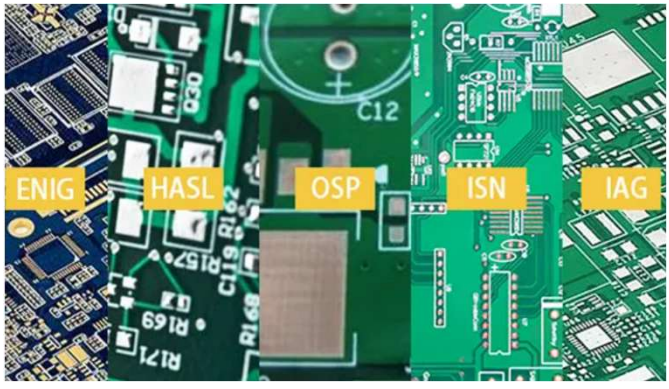
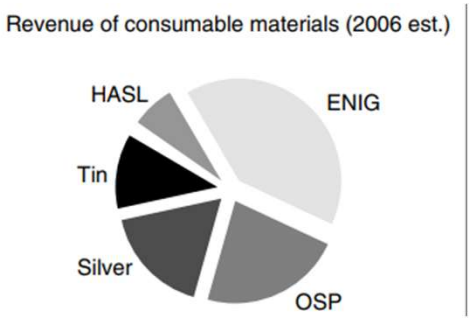
Surface Finish



Surface Finish Aspect



Surface Finish Repartition

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Surface Finish

	IPC-6012 HASL	IPC-6012 OSP	IPC-4553A Imm Silver	IPC-4554 Imm Tin	IPC-4552A ENIG	IPC-4556 ENEPIG
Planarity	No	Yes	Yes	Yes	Yes	Yes
Solderjoint	Cu-Sn	Cu-Sn	Cu-Sn	Cu-Sn	Ni-Sn	Ni-Sn
Relative Cost	$	$	$$	$$	$$$	$$$
IPC Shelf Life	No Specification	No Specification	12 months	12 months	12 months	12 months
Reflows	6	4	6	2	6	6
Contact	E-Test, ICT	Difficult	E-Test, ICT, Keypad	E-Test	E-Test, ICT, Keypad	E-Test, ICT, Keypad
Press Fit	Good	Good	Good	Good	Good	Good
Au Wirebond	No	No	No	No	No	Yes
Al Wirebond	No	No	Yes	No	Yes	Yes

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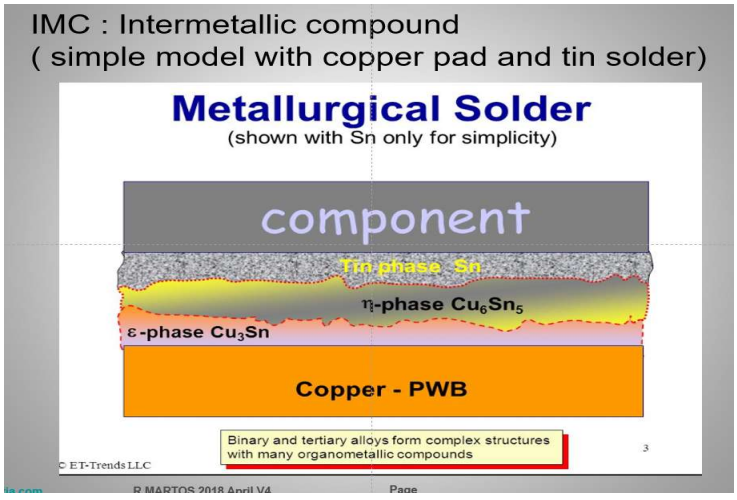
Surface finish of a PCB

SMT soldering and Wave soldering = Building an IMC



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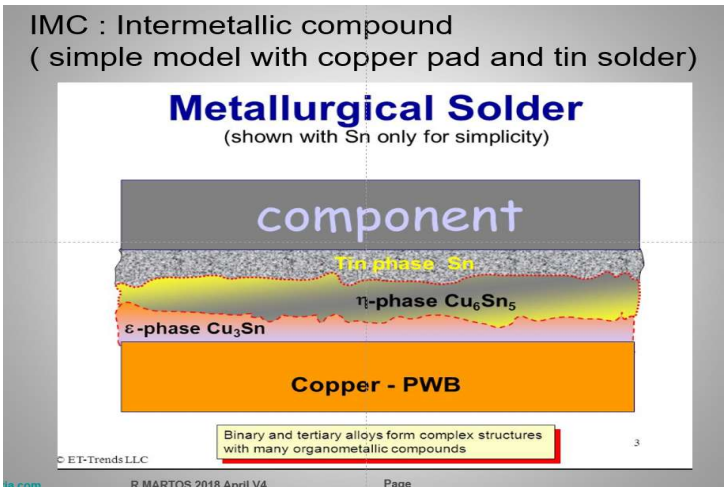
IMC (intermetallic compound)



- Tin very found of Copper !!
(and of Nickel also)
- Tin is very found of cristallographic growth (alone)
- Tin Atom is very mobile

Whatever PCB surface finish, whatever solder paste, Tin will always be present !!

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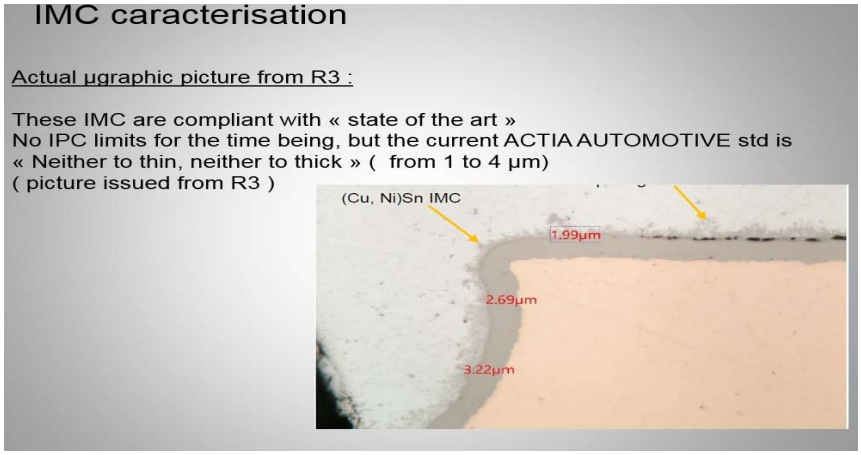

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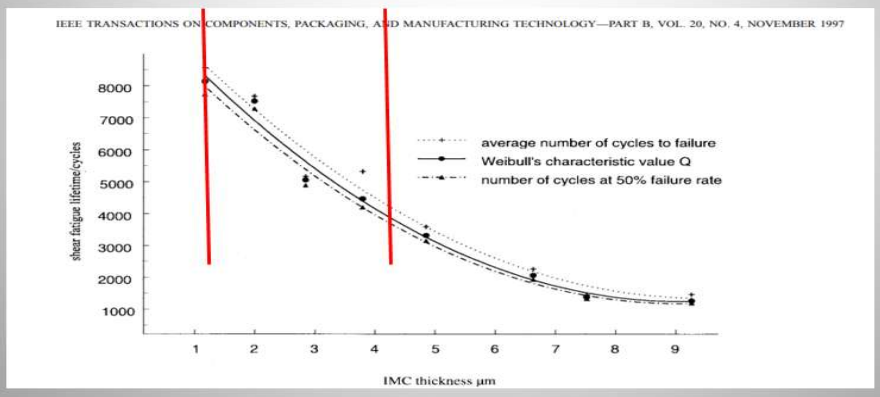
IMC caracterisation (con't)

Why our IMCs are optimized versus the lifetime of shear stress fatigue:

(Actia Spec thickness: 1 to 4 µm for SnxNiy)
Current value for these balls (2 to 3,2 µ)



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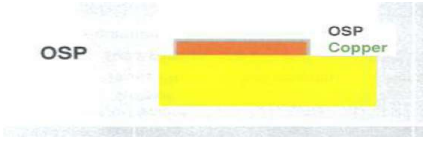
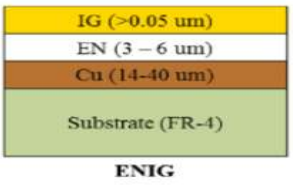
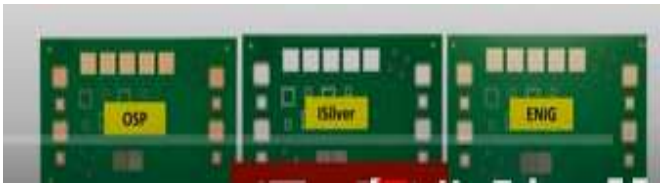
Surface finish of a PCB

OSP ImTin ENIG





Conventional Reflow Plating



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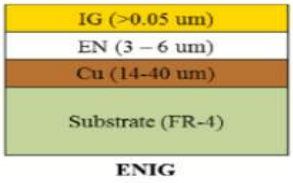
ENIG



ENIG

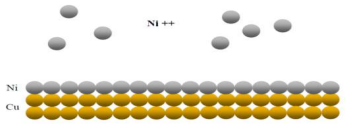
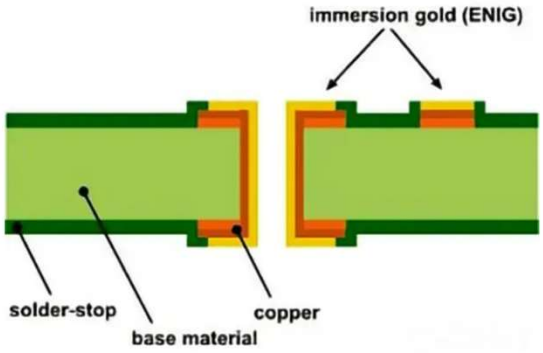


Figure 2.1: Electroless Nickel Plating



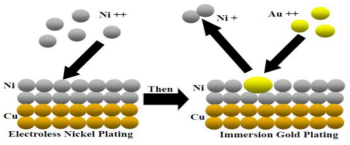


Figure 2.2: Electroless Nickel / Immersion Gold Plating

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Black Pad On ENIG process

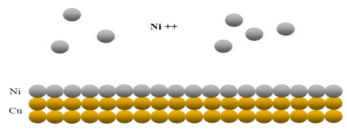


Figure 2.1: Electroless Nickel Plating

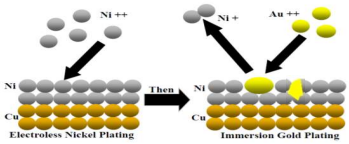


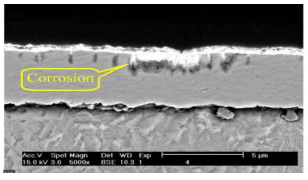
Figure 2.2: Electroless Nickel / Immersion Gold Plating

Ni Thickness : 5 µ
Au Thickness : 50 nm
IPC 4552

Immersion gold on Nikel plating is a violent oxydo reduction reaction (substitution)

Phosporus in Nikel to quiet the reaction
Not enough P ➔ Nikel too oxidized ➔ Black Pad (hyper oxidation/Corrosion)
Too much P ➔ Sn will not come in substituion to build IMC

6 % < P < 14 %



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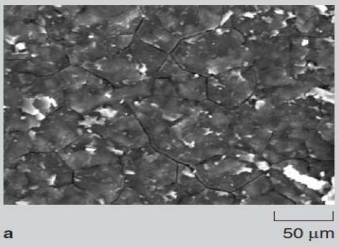
Black Pad On ENIG process

No solder visible on the pad (all on the cpt side)
The pad surface appeared « black » and clean

The root cause is the % of Phosporus in the Nickel
Too few ➔ oxydation of the Nickel beneath the gold
Too much ➔ the phosporous atoms prevent the diffusion of the Sn atoms

Should be between 6 and 14 %

ENIG plating is not so trivial ! .
Must be controled
Less and less issue than in the past with major suppliers



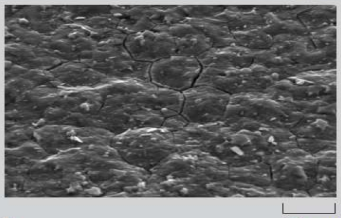


Figure 2. (a) The top view and (b) side view of mud-cracks in the entire pad surface.

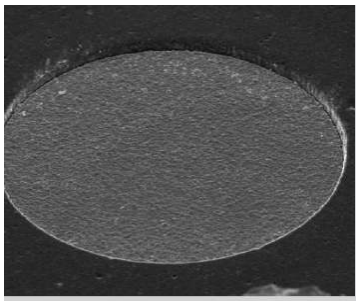


Figure 1. A 30-degree tilt view of a black pad. The pad surface appeared clean. Only a small amount of fine IMC particles (gray) and little solder residue were present on the pad.

R.M.E.

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R.M.E.

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R.M.E.

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OSP
Drawbacks

A-1 : OSP thickness (4/24 µ inches (100/600 nm)
➔ Thickness measurment (Supplier)
(too thick ➔ diff to solder , too thin ➔ not enough protection)

A-2 : Nber of thermal excursion (naked copper will oxydize)

A-2.1 : Backing not recommended
A-2.2 : PTH selective soldering issue
A-2.3 : Test pad to be soldered (ICT issue)

See IPC 2221 :

Quand vous choisissez l'OSP comme finition de surface, il est conseillé de travailler avec l'assembleur pour confirmer que les conditions d'assemblage (par exemple, le nombre et le type de cycles de refusion, les temps d'attente en cours de procédé) sont compatibles. Certaines conceptions ne conviennent pas aux OSP. Les fabricants n'utilisent souvent qu'un seul produit OSP, donc spécifier un OSP peut limiter le choix des fournisseurs.

R.M.E.

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OSP
Drawbacks

A-3 : Chemix
A-3.1 : cleaning on mis printed Boards to forbid
A-3.2 : packing and handling
Sliding on each other will scratch the OSP layer on PCB ➔ forbid move (inside packing and during loading/ unloading, interleave paper ?)
Gloves mandatory !

R.M.E.

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ImTin
Drawbacks

A-1 : **IMC growth all along the thermal process**

There is already an IMC at initial ImTin
IMC grows even at 25 ° (exponent for temp, square root for duration)
The more important growth is the top side during the first reflow (the other side is less sentive because the Tin is alloyed (SAC) .
The more IMC grows the more Tin is consumed and so offers less protection to copper inducing solderability issue .

R.M.E.

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ImTin
Drawbacks

- A-2 Tin Chemix

- A-2.1 : Whiskers

As soon as solder paste is deposit, less whiskers issue risk
Ask for a special chemix with a low amount of Silver in Tin (goal is to quiet Tin)
➔ Ie Stanatech 2000 from ATO

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FRAMATECH

CYCLE : Performance électronique

LES EXIGENCES DE L'IPC A 600

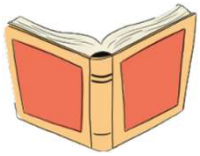
Partie B

Les critères d'acceptation essentiels

FRAMATECH S.A. au capital de 38112 Euros
Etudes & mises en œuvre de stratégies industrielles internationales Hautes Technologies

4 boulevard d'Arras - 13004 Marseille - France
Tél. +33 491 95 55 70 | Mail : contact@framatech.fr
Organisme de formation n° 93060115506 | Siret 344 351 879 00046 | NAF 742C
Web : www.framatech.fr

Partie B :
Les critères d'acceptation essentiels



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1.4 Classification

Classe 1 – Produits Electroniques Généraux

Comprend les produits pour des applications où l'exigence principale est le fonctionnement de l'ensemble électronique terminé.

Classe 2 – Produits Electroniques Spécialisés

Inclus des produits nécessitant des performances élevées et une longue durée de vie pour lesquelles un fonctionnement ininterrompu est souhaitable, mais non critique. Typiquement le milieu de l'utilisation ne causerait pas de panne.

Classe 3 – Produits Electroniques Haute Performance

Inclus les équipements et produits pour lesquels un bon fonctionnement continu et sur demande est critique, pour lesquels on ne peut pas tolérer d'interruption du fonctionnement du matériel. L'environnement d'utilisation peut être particulièrement difficile et le fonctionnement doit être toujours assuré. C'est le cas des dispositifs de survie ou autres systèmes critiques.

	IPC Classe 1	IPC Classe 2	IPC Classe 3
Catégorie	Electronique générale	Electronique de service dédiée	Electronique haute fiabilité
Cycle de vie	Court	Long	Très long
Qualité	Basse	Bonne	Infaillible
Exemples	Jouets, Lampes de poche, Smartphones	Ordinateurs portables, micro-ondes, switchs	Aérospatial, Militaire et applications médicales

2

2

1.6 Documents applicables

J-STD-003 Solderability Tests for printed boards
IPC-T-50 Terms and définition (see extract)
IPC-TM-650 Test methods manual (free)
2.1.1 Microsectionning method
2.2.2 Optical dimension verification
2.3.25 Detection and measurment of ionizable surface contaminants
2.4.1 Adhesion, tape testing
2.4.22 Bow and twist
2.4.28.1 Adhesion, solder mask, tape test method
2.6.8 Thermal Stress, Plated-Through Holes
2.6.25 CAF (Conductive Anodic Filament) testing and resistance Test (ECM)
IPC-SM-840 Qualification and performance of Solder Mask
IPC-2220 Family of design document
IPC-4562 Metal foil for printed board
IPC-6012 Qualification des performances des Circuits imprimés rigides
NB : l'IPC 6012 est aussi un document à croiser avec l'IPC 600 (complément très utile)

IPC-6013 Qualification des performances des Circuits imprimés flexibles

3

3

1.8 Termes et définitions : ➔ IPC-T-50
See extract

4

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1.10 Fabrication

1.10 FABRICATION

Les circuits imprimés fabriqués selon les exigences de ce document **doivent** l'être de telle façon qu'ils soient uniformes en qualité et que soit évitée la présence de poussières, de matériaux étrangers, de graisse, d'empreintes digitales, de résidus de flux ou d'autres contaminants qui pourraient affecter la durée de vie et l'utilisation du produit. Les circuits imprimés **ne doivent pas** comporter plus

L'Environnement de stokage et de travail doit etre contrôlé :

- Temperature
- Humidité (cf datasheet des matière)
- Particules (classe ISO 14644)

Numéro de classification	Concentrations maximales admissibles (particules/m³ d'air) en particules de taille égale ou supérieure à celle donnée ci-dessous					
ISO (N)	0,1 µm	0,2 µm	0,3 µm	0,5 µm	1 µm	5 µm
Classe ISO 1	**10**	d	d	d	d	e
Classe ISO 2	**100**	**24**[b]	**10**[b]	d	d	e
Classe ISO 3	**1 000**	**237**	**102**	**35**[b]	d	e
Classe ISO 4	**10 000**	**2 370**	**1 020**	**352**	**83**[b]	e
Classe ISO 5	**100 000**	**23 700**	**10 200**	**3 520**	**832**	d, e, f
Classe ISO 6	**1 000 000**	**237 000**	**102 000**	**35 200**	**8 320**	**293**
Classe ISO 7	c	c	c	**352 000**	**83 200**	**2 930**
Classe ISO 8	c	c	c	**3 520 000**	**832 000**	**29 300**
Classe ISO 9[g]	c	c	c	**35 200 000**	**8 320 000**	**293 000**

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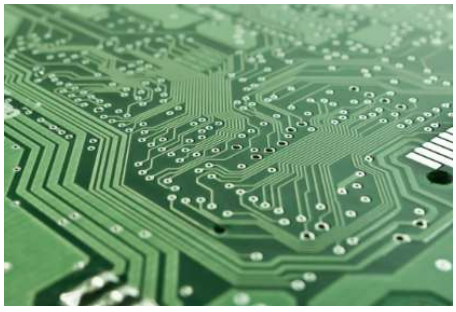
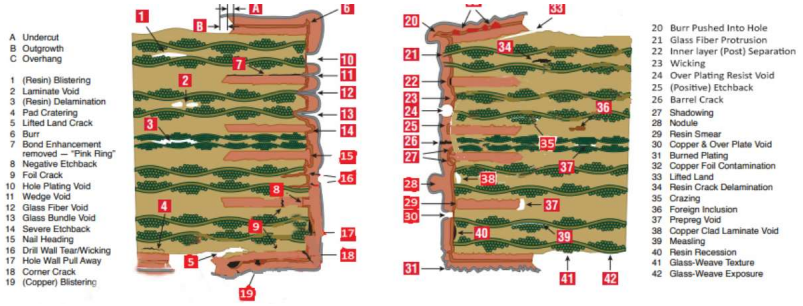
2 Caractéristiques observables de l'extérieur
3 Caractéristiques observables en interne



Extérieur



Cross section

80 % des problemes en PCB, ne sont visibles qu'en interne !!

6

6

2.1 Bord des circuits imprimés

1. Bavures non métalliques

2. Bavures metalliques

Acceptable – Class 1, 2, 3
- Edges are rough but not frayed.
- Nicks do not extend more than 50% of the distance from the edge of the board to the closest conductor or are greater than 2.5 mm [0.0984 in] whichever is less.

3. Entailles

Acceptable – Class 1, 2, 3
- Penetration of haloing does not reduce the unaffected distance from the board edge to the closest conductive pattern by more than 50% or more than 2.5 mm [0.0984 in], whichever is less.

4. Haloing

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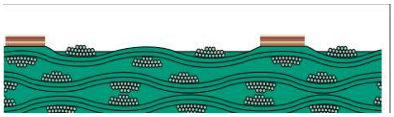
2.2 Surface du matériau de base

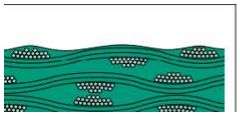
Critères très specieux car le Solder mask les rend innaprop

2.2.1 Tissu exposé



Acceptable – Class 1, 2, 3
- Excluding the area(s) with weave exposure, the remaining space between conductors meets the minimum conductor spacing requirement.

2.2.2 Tissu apparent

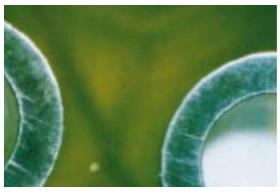


Acceptable – Class 1, 2, 3
- Weave texture is an acceptable condition in all classes but is sometimes confused with weave exposure because of similar appearances.

2.2.3 Fibres exposées/cassées

Critère très flou

2.2.4 Vides de surface



Acceptable – Class 1, 2, 3
- Pits or voids do not exceed 0.8 mm [0.031 in].
- Total board area affected is less than 5% per either side
- Pits or voids do not bridge conductors.

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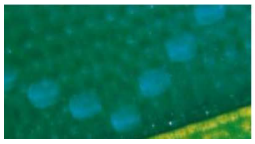
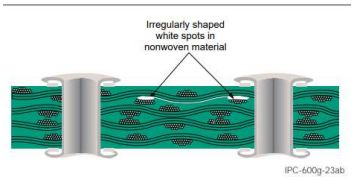
2.3 Sous la surface du matériau de base

2.3.1 Point de couleur claire (measling)



Acceptable – Class 1, 2, 3

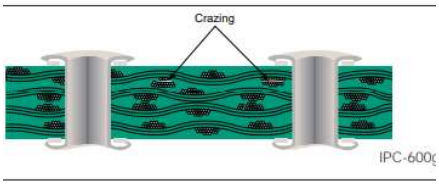
- Measles are acceptable for all products, except for high-voltage applications as defined by the customer.



2.3.2 Traces de couleur claire dans le tissage

Acceptable – Class 2, 3

- The imperfection does not reduce the space between conductive patterns below the minimum conductor spacing.
- The distance of crazing does not span more than 50% of the distance between adjacent conductive patterns that are not electrically common.



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2.3.3 Delamination

Figure 233c

Acceptable – Classe 3, 2

- La surface affectée par l'anomalie n'excède pas 1% de la surface du circuit sur chaque face.
- L'anomalie ne réduit pas les isolements entre conducteurs en dessous de la distance minimum entre conducteurs.
- Le cloquage ou délaminage ne s'étend pas sur plus de 25% de la distance entre éléments conducteurs adjacents.
- Pas de propagation suite aux tests thermiques qui simulent les procédés de fabrication.
- L'anomalie ne réduit pas la distance minimum spécifiée entre le bord du circuit et les conducteurs ou ne doit pas excéder 2,5 mm [0.0984in] si rien n'est spécifié.

2.3.4 Inclusion de FOD

Acceptable – Class 1, 2, 3

- Translucent particles trapped within the board **shall** be acceptable.
- Opaque particles trapped within the board **shall** be acceptable provided the particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified in the IPC-6010 series.
- Electrical parameters of the board are unaffected.

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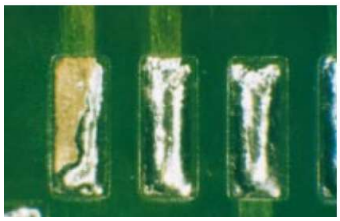
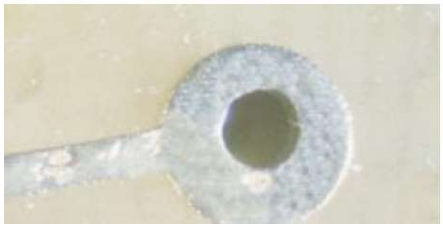
2.4.1 Finition HAL (Obsolete) non Wetting



Nonconforming – Class 1, 2, 3
• Defects either do not meet or exceed above criteria.

Critère 100 %

2.4.2 Finition HAL De Wetting



Acceptable – Class 2, 3
• On conductors and ground or voltage planes.
• On 5% or less of each land area for solder connection.

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2.5 Trous metallisés

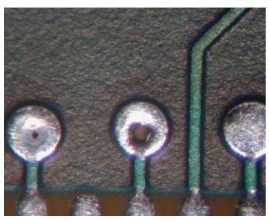
2.5.1 Nodules
2.5.2 Anneau rose (Pink ring)
2.5.3 Manques Cuivre
2.5.4 Manques finition

Trop spécifiques ou obsoletes

2.5.5 Manques finition

Nonconforming - Class 1, 2, 3
• Defects either do not meet or exceed above criteria.

2.5.6 Metallisation de couverture des vias (cap plating



Nonconforming - Class 1,2,3（不符合条件 - 1,2,3级）
• Defects either do not meet or exceed above criteria.
• 缺陷不符合或超出上述要求。

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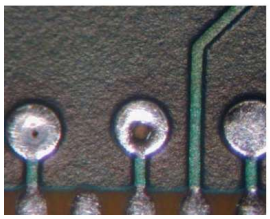
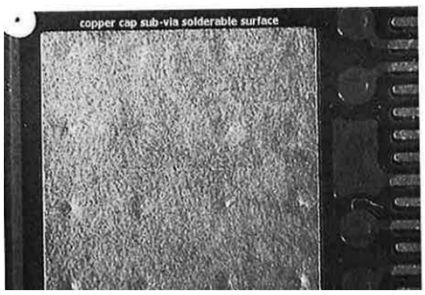
2.5.6 Metallisation de couverture des vias (cap plating



Nonconforming - Class 1,2,3（不符合条件 - 1,2,3级）
• Defects either do not meet or exceed above criteria.
• 缺陷不符合或超出上述要求。



Acceptable – Classe 3, 2, 1

- Lorsque la métallisation de couverture des trous via remplis est spécifiée sur les documents d'approvisionnement, les exigences selon 2.7.1.1, 2.7.1.2, 2.7.1.3 et celles relatives à la spécification applicable pour les pastilles de montage en surface rectangulaires et rondes **doivent** s'appliquer.
- Pas de manque dans la métallisation laissant la résine de remplissage apparente, à moins que celle-ci soit couverte par le vernis épargne de brasage.
- Protubérances (bumps) et/ou enfoncements (dimples) visibles qui satisfont aux exigences d'intégrité structurelle de la spécification de performance applicable.

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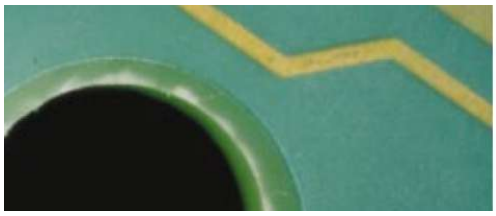
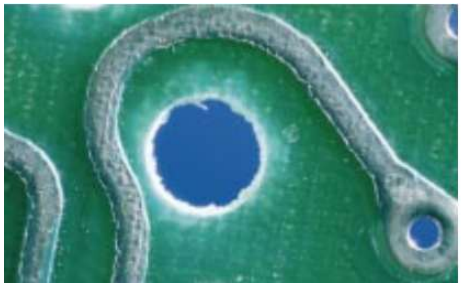
2.6 Trous non metallisés

2.6.1 Eclatement de la résine (Haloing)



Acceptable – Class 1, 2, 3

- Penetration of haloing does not reduce the unaffected distance from the board edge to the closest conductive pattern by more than 50% or more than 2.5 mm [0.0984 in], whichever is less.



Nonconforming – Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

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2.7 Contacts en surface

Non traité
Critères très spécifiques (voir le doc IPC A 600)

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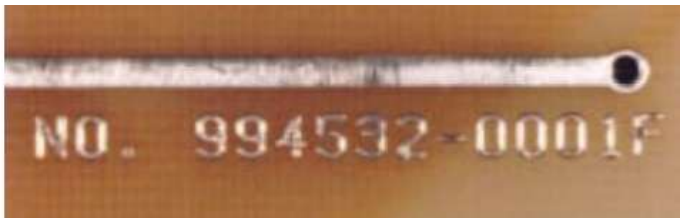
2.8 Marquage

Non traité
Critères très spécifiques ou obsoletes



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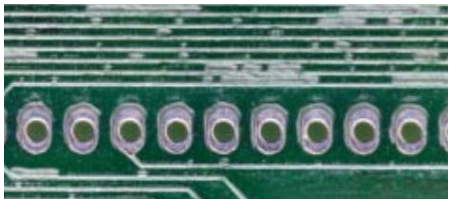
2.9 Vernis epargne (Solder mask)

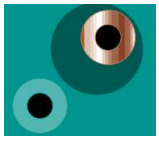
2.9.1 Recouvrement des conducteurs

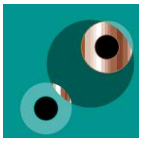
Manque de vernis entre 2 pistes conductrice



2.9.2 décalage par rapport aux trous

Pas de solder mask dans les PTH
Les pads ou trous de potentiel de potentiel différents
ne sont pas découvert





OK NOK

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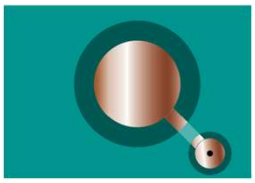
2.9.3.3 Décalage par rapport aux pastilles rondes BGA
(barriere de soudure) (DAM)



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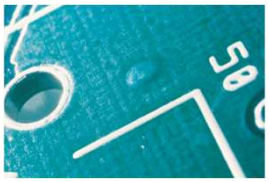
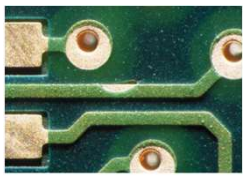
2.9.4 Cloquage/ delamination



Acceptable – Classe 3, 2

- Deux cloques ou deux délaminages par face n'excédant pas 250 µm [9.843 µin] dans leur plus grande dimension.
- La réduction de l'isolement électrique due aux cloques ou au délaminage n'excède pas 25%, ou la valeur minimum.

2.9.5 Adherence (Peeling)



Acceptable – Classe 3, 2

- Pas de décollement visible du vernis épargne sur la surface du circuit imprimé avant test.
- Les éclats ou le décollement du vernis épargne le long du bord du circuit imprimé ne pénètrent pas de plus de 1,25 mm [0.050 in] ou 50% de la distance du conducteur le plus proche, le plus petit des deux s'applique, quand le design (définition du cheminement électrique) exige le recouvrement du bord du circuit.

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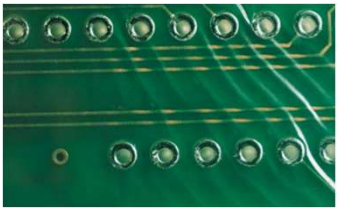
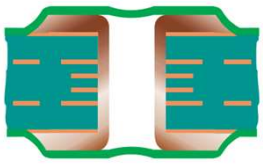
2.9.6 Vagues/ Rides

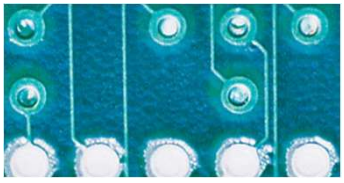


Acceptable – Classe 3, 2, 1

- Les vagues et ondulations dans le vernis épargne ne réduisent pas son épaisseur en dessous du minimum spécifié (si spécifié).

2.9.7 Tenting





Acceptable – Class 3, 2, 1

- Tous les trous devant être bouchés sont complètement couverts par ce masque.

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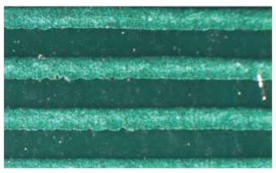
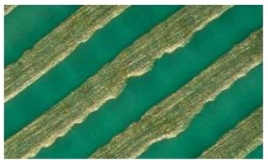
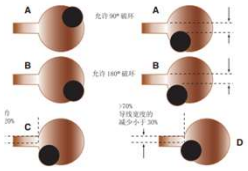
2.10.1.1 Largeur des pistes conductrices



2.10.1.2 Largeur des isolements



2.10.2 / 2.10.3 / 2.10.4 Collerette (voir critère)



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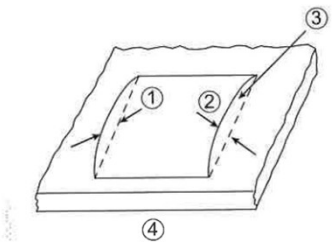
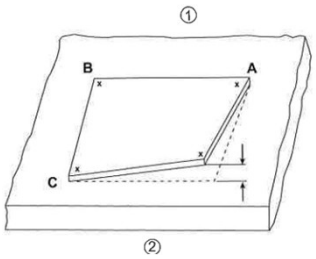
2.11 Planeité (Bow and Twist)
Mesure selon l'IPC TM 650 method 2.4.22

Accept : 0,75 %





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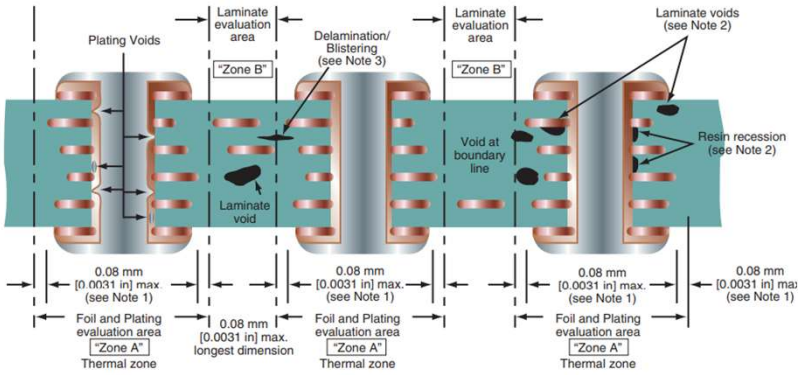
3 Caractéristiques observables en interne (donc microsection)

Définition Zone Thermique vs
Hors zone thermique (+80 um autour de la verticalité d'un trou avec cuivre)



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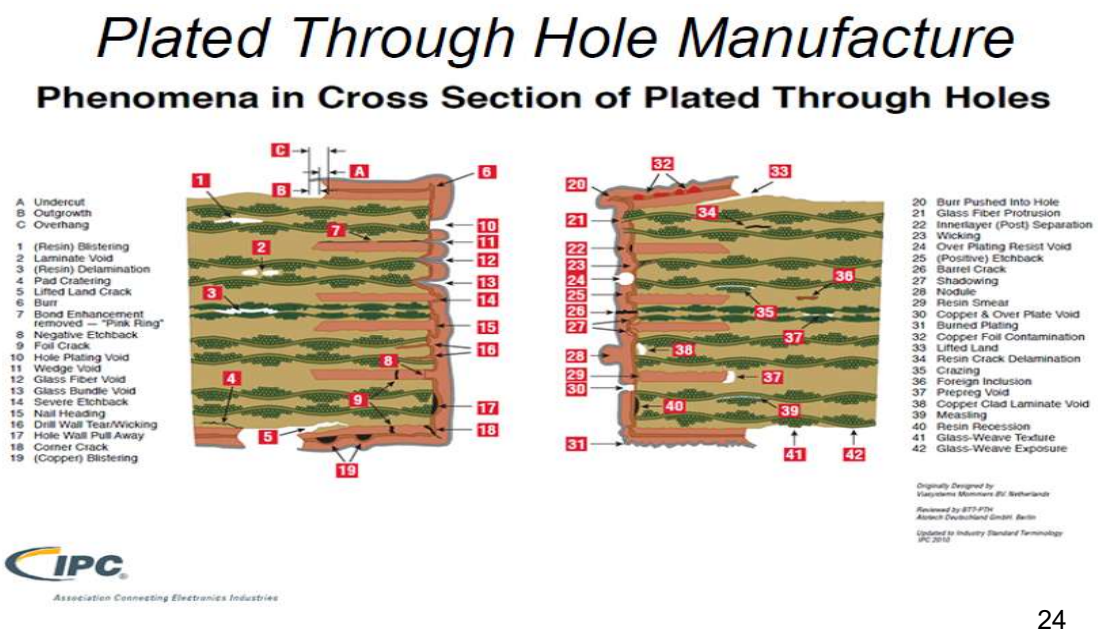
3 Caractéristiques observables en interne (donc microsection)



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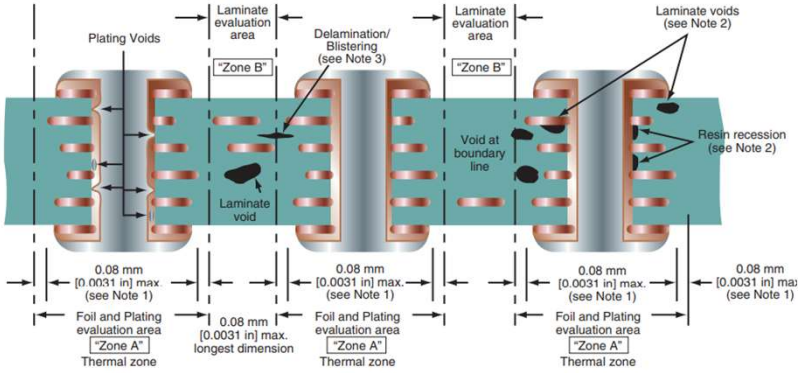
3 Caractéristiques observables en interne (donc microsection)

Définition Zone Thermique vs
Hors zone thermique (+80 um autour de la verticalité d'un trou avec cuivre)



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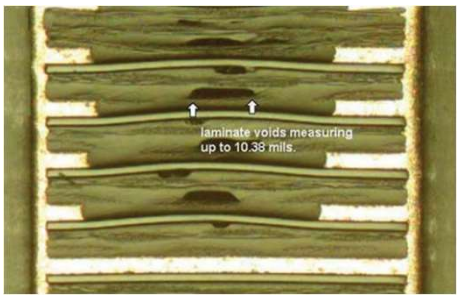
3.1.1 Cavités, délamination en dehors des zones thermiques
Les critères concernant les zones thermique seront vu plus loin

Critère 150 um

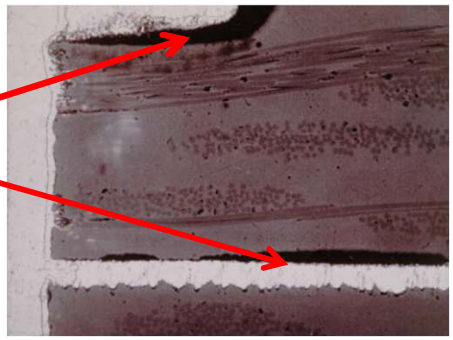


26

26

3.1.4 Délamination/Cloquage

Pas de délamination ou cloquage visible



3.1.6 Retrait de resine

(Critère mal défini , car il s'agit en fait d'un smearing de resine, qui n'a pas été « désmearé » chimiquement .

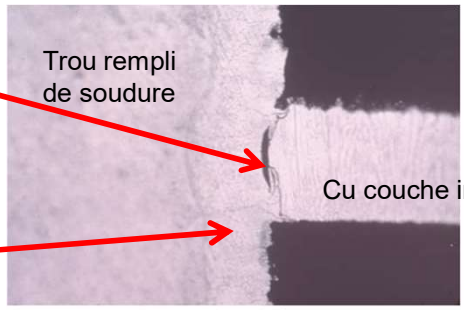


Figure 315a An Example of Resin Smear

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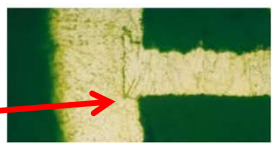
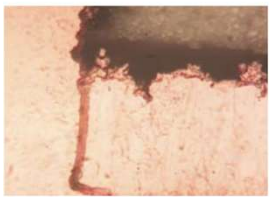
3.1.5 Etchback

Positive Etchback

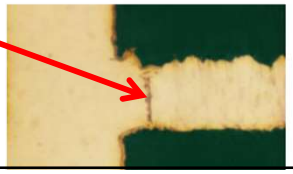


Target Condition – Class 1, 2, 3
- Uniform etchback to a preferred depth of 0.013 mm [0.000512 in].



Acceptable – Class 1, 2, 3
- Etchback between 0.005 mm [0.00020 in] and 0.08 mm [0.0031 in].
- Shadowing is permitted on one side of each land.

Negative Etchback



Acceptable – Class 3
- Negative etchback less than 0.013 mm [0.000512 in].

Acceptable – Class 1, 2
- Negative etchback less than 0.025 mm [0.000984 in].

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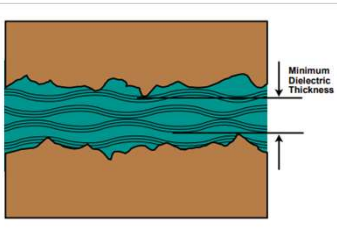
3.1.7 Espacement entre couche



Target Condition – Class 1, 2, 3

- The minimum dielectric thickness meets the requirements of the procurement documentation.

Acceptable – Class 1, 2, 3

- The minimum dielectric thickness meets the minimum requirements of the procurement documentation. If not specified, must be 0.09 mm [0.0035 in] or greater.

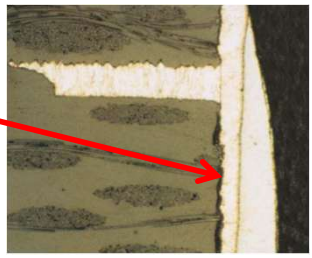
Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

3.1.8 Retreint de résine

Acceptable – Classe 3, 2, 1

- Le rétreint de résine est acceptable après les tests de stress thermique.



29

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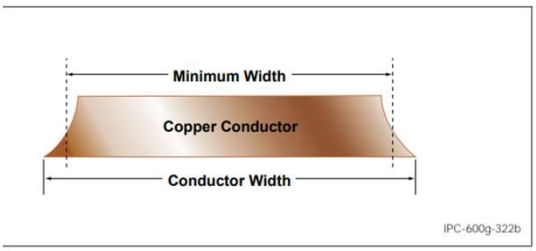
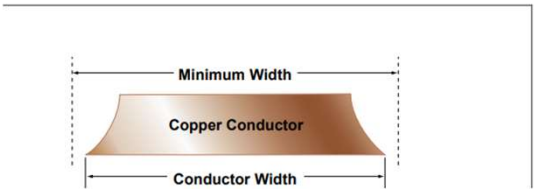
3.2.1 Caractéristiques de gravure
3.2.2 Imprimer et graver



Acceptable – Class 1, 2, 3

- Conductor width meets minimum requirement.



Nonconforming - Class 1, 2, 3

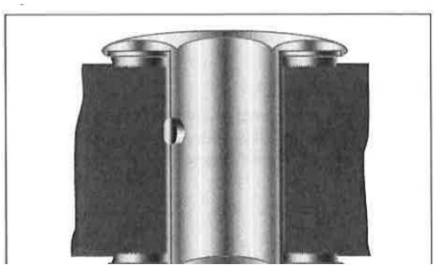
- Defects either do not meet or exceed above criteria.

30

30

3.3 Trous métallisés

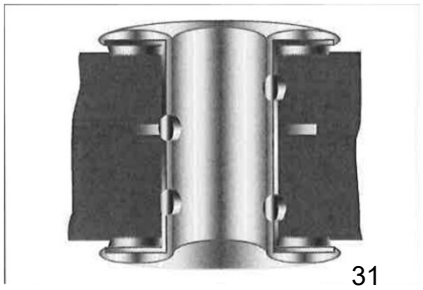
3.3.1 Manque dans la metallisation



Acceptable – Classe 3, 2

- Pas plus d'un manque dans la métallisation par coupon test ou par circuit imprimé, quelle que soit leur longueur ou leur taille.
- Pas de manque dans la métallisation plus grande que 5% de l'épaisseur totale du circuit imprimé.
- Pas de manque visible dans la métallisation à l'interface d'une couche interne et de la paroi du trou métallisé ou du microvia.
- Manques dans la métallisation inférieurs ou égaux à 90° de la circonférence du trou.

3.3.1 Manque dans la metallisation



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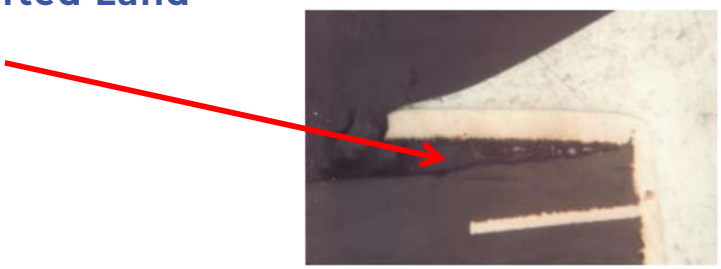
3.3.2 Lifted Land



Acceptable – Class 1, 2, 3

After thermal stress testing or rework simulation:

- Lifted lands are allowed.

Interpretation : Non acceptable donc avant thermal stress .
Après thermal stress, il vaudrait mieux appliquer le critère de l'IPC A610
(à savoir limite de l'epaisseur du cuivre)

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3.3.3 Plis dans la métallisation

Critère très spécieux

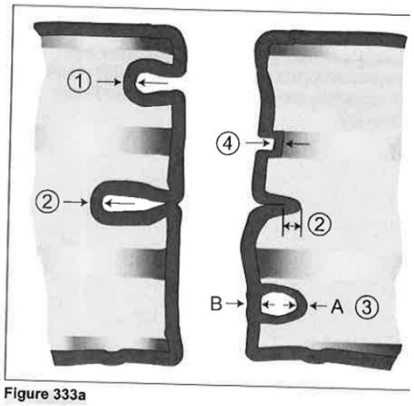
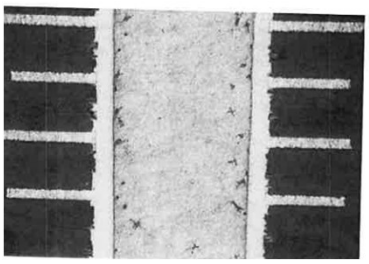


Figure 333a

Note 1 : Point de mesure de la métallisation de cuivre minimum. Les plis dans la métallisation qui ne sont pas fermés et dont l'épaisseur minimum de métallisation de cuivre respecte les exigences de l'IPC-6010 sont acceptables.
Note 2 : Plis dans la métallisation fermés (inclusions) avec une ligne de délimitation visible. Mesure et acceptation selon Note 1.
Note 3 : Pli dans la métallisation fermé sans ligne de délimitation visible. La mesure de l'épaisseur A+B **doit** être conforme à l'épaisseur minimum de métallisation de cuivre selon la série des IPC-6010.
Note 4 : Point de mesure de la métallisation de cuivre minimum pour le retrait négatif de résine (negative etchback).

Rappel : la métallisation des trous/vias doit se rapprocher de cela



Objectif – Classe 3, 2, 1

- La métallisation est lisse et uniforme tout au long du trou. Pas de pliures ou d'inclusions visibles.

33

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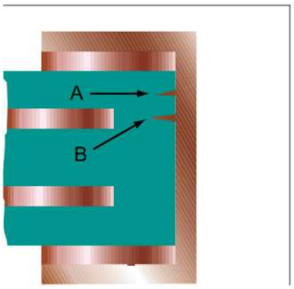
3.3.4 Infiltration de la métalisation (Wicking)



Acceptable – Class 1, 2, 3

- Wicking (B) does not reduce spacing less than specified minimum on the procurement documentation.

Acceptable – Class 3

- Wicking (A) does not exceed 80 µm [3,150 µin].

Acceptable – Class 2

- Wicking (A) does not exceed 100 µm [3,937 µin].

Acceptable – Class 1

- Wicking (A) does not exceed 125 µm [4,291 µin].

3.3.5 Plating Crack (Barrel)

Target Condition – Class 1, 2, 3

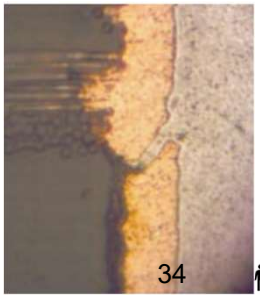
- Barrel plating is free of cracks.

Acceptable – Class 1, 2, 3

- No cracks in plating.

Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.



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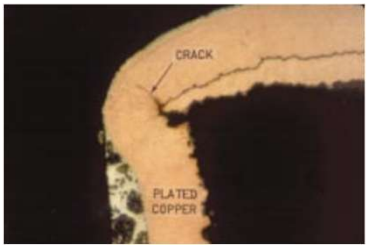
3.3.6 Plating Crack (corner)



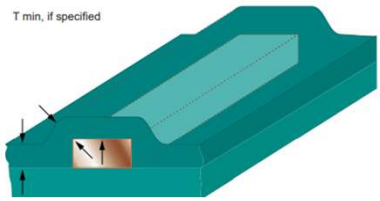
Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

35

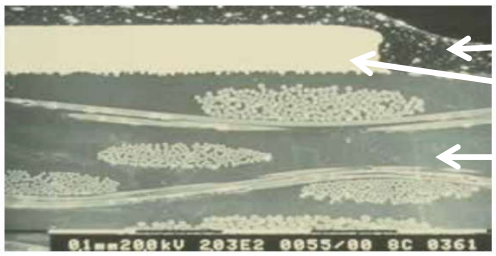
35

3.3.11 Solder coating thickness



Acceptable - Class 1, 2, 3

- Specified: The solder resist thickness meets the thickness requirements on the procurement documentation (cannot be visually assessed).



Solder Mask

Copper track

Pre Preg

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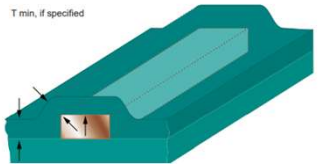
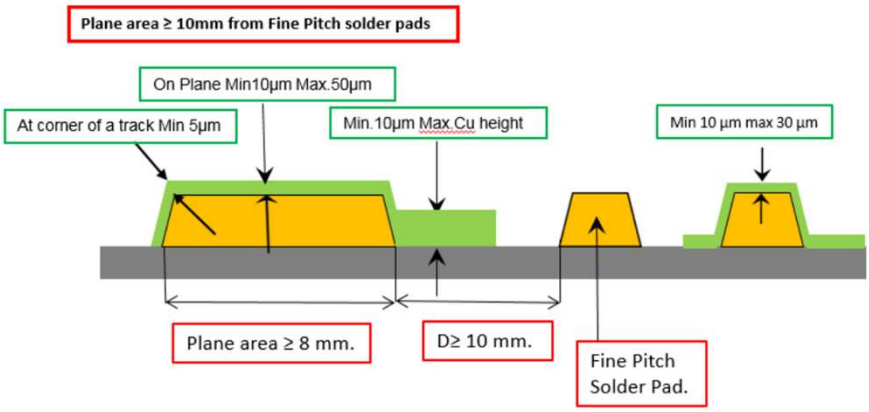
3.3.11 Solder coating thickness



Acceptable - Class 1, 2, 3

- Specified: The solder resist thickness meets the thickness requirements on the procurement documentation (cannot be visually assessed).

IPC A 600



IPC A 6012
Qualification et performances des Circuits imprimés rigides

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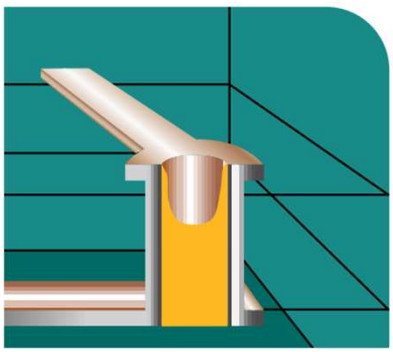
3.3.15 Material fill of blind and burried vias



Acceptable - Class 2, 3

- At least 60% buried via fill with laminating resin or similar via fill material.

Acceptable - Class 1

- Buried vias completely void of fill material.

Nonconforming - Class 1, 2, 3

- Defects either do not meet or exceed above criteria.

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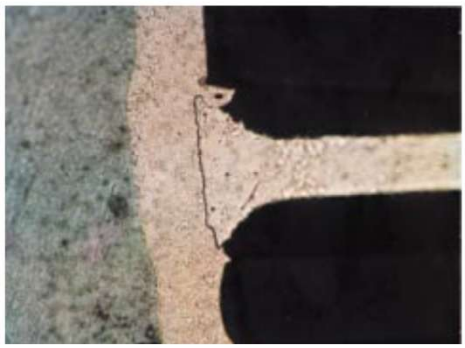
3.4.2 Nail Heading (effet tête de clou)

No evidence exists that nail heading affects functionality. The presence of nail heading may be considered an indicator of process or design variation but is not a cause for rejection. Consider evaluation for glass bundle damage.



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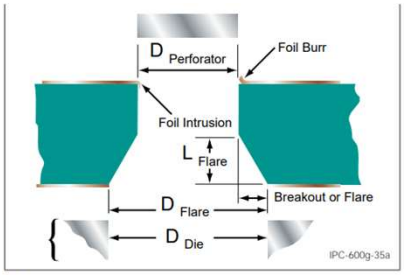
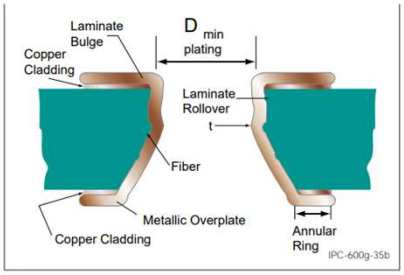
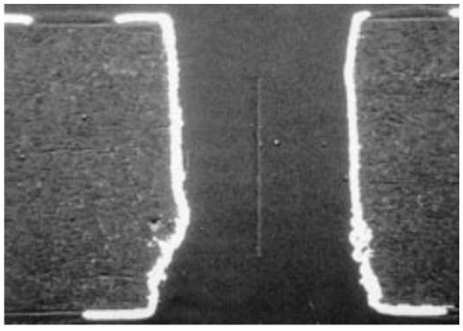
3.5 Plated Through Hole –Punch process



Punched



Punched and Plated



Acceptable – Class 1, 2, 3

- Roughness or nodules do not reduce plating thickness or hole diameter below minimum requirements.

40

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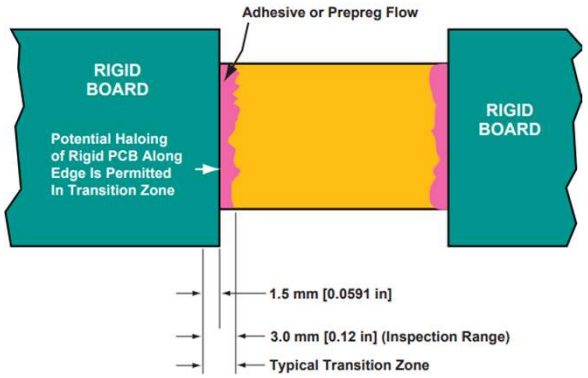
4.1 Flexible and Rigid flex PCB

Non traité, car spécifique au procédé flex rigid

CF: Qualification and Performance Specification
for Flexible/Rigid-Flexible Printed Boards



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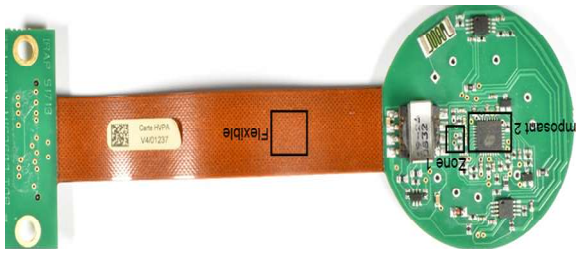
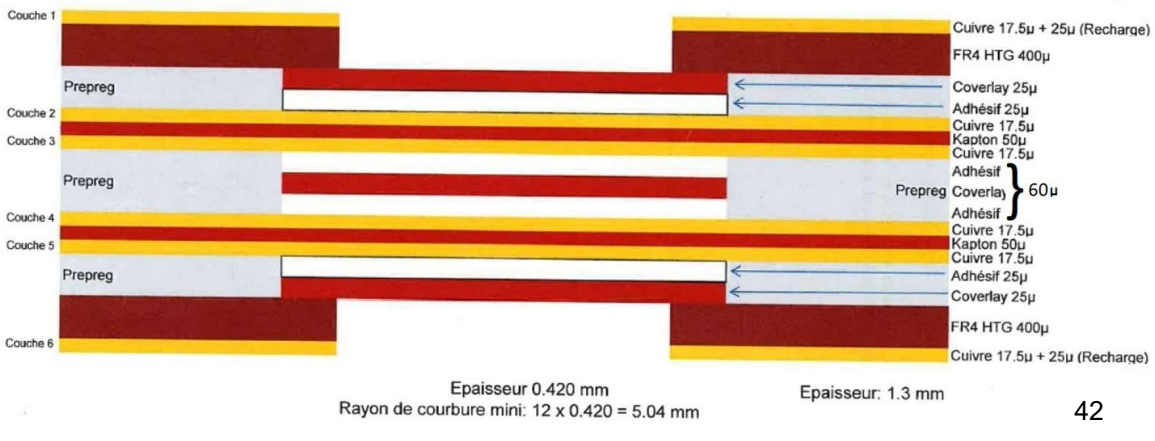
4.1 Flexible and Rigid flex PCB





Epaisseur 0.420 mm
Rayon de courbure mini: 12 x 0.420 = 5.04 mm

Epaisseur: 1.3 mm

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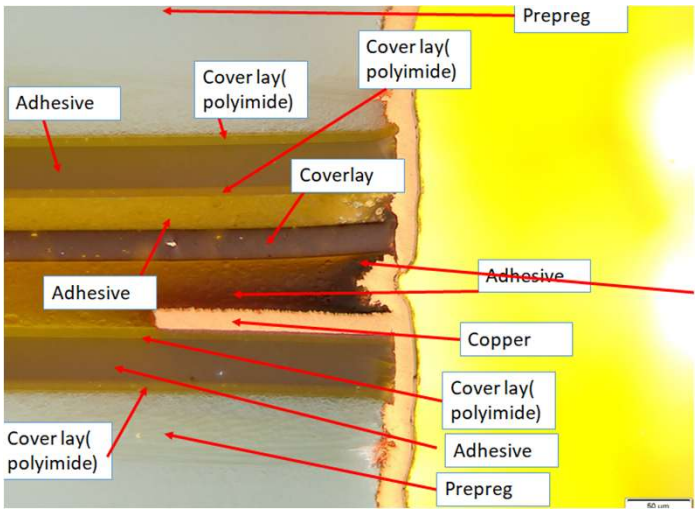
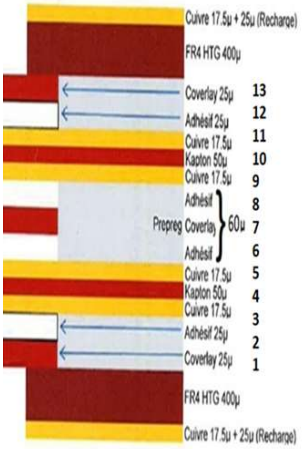
4.1 Flexible and Rigid flex PCB





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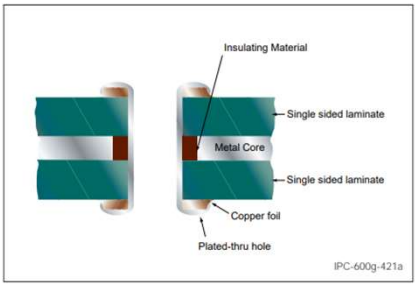
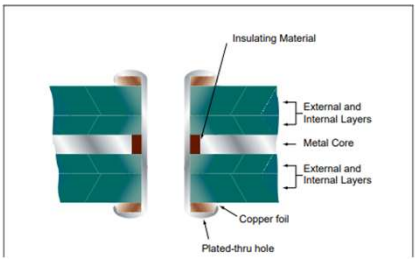
4.2 Metal Core Printed Board



Laminated Type Metal Core Board

- Single conductive layer on both sides and insulated from the metal core substrate. Conductive material to be copper foil and electrodeposited copper.



Laminated Type Metal Core Multilayer Board

- More than one conductive layer on one or both sides and insulated from the metal core substrate. Conductive material to be copper foil and electrodeposited copper.

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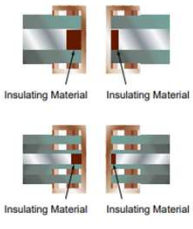
4.2 Metal Core Printed Board

Critères identiques au PCB rigides , avec en sus….

Spacing 100 um

Two Sided

Multilayer



Acceptable – Class 1, 2, 3

- The spacing between the metal core and the plated-through hole or the metal core and adjacent conductive surfaces is greater than 0.1 mm [0.0040 in].

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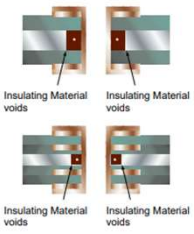
4.2 Metal Core Printed Board

Critères identiques au PCB rigides , avec en sus….

Voids or resin recession
(100 um criterion or AABUS)

Two Sided

Multilayer



Acceptable – Class 1, 2, 3

- Insulating material meets minimum thickness and dielectric spacing requirements.
- Voids or resin recession does not cause spacing to be less than acceptability requirements.

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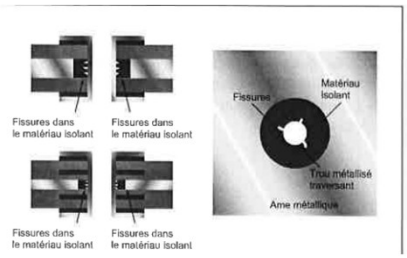
4.2 Metal Core Printed Board

Critères identiques au PCB rigides , avec en sus….

Vicking et/ou fissures :
Isolement doit rester > 100 um

Vicking et/ou fissures < 75 um



Acceptable – Classe 3, 2, 1

- Les infiltrations de la métallisation (wicking), des fissures radiales, l'isolement latéral ou des manques dans le matériau de remplissage isolant ne réduisent pas l'isolement électrique entre les surfaces conductrices adjacentes à moins de 100 µm [0.003937 in].
- Les infiltrations de la métallisation (wicking) et/ou des fissures radiales n'excèdent pas 75 µm [0.00295 in] à partir du bord du trou dans le matériau de remplissage isolant.

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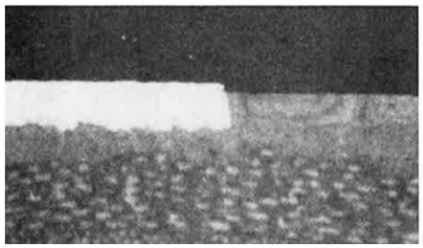
4.3 Flush Printed Board (conducteur encastré)

Le non affleurement
est donc AABUS



Acceptable – Classe 3, 2, 1

- Le conducteur n'est pas affleurant mais respecte les exigences minimum.

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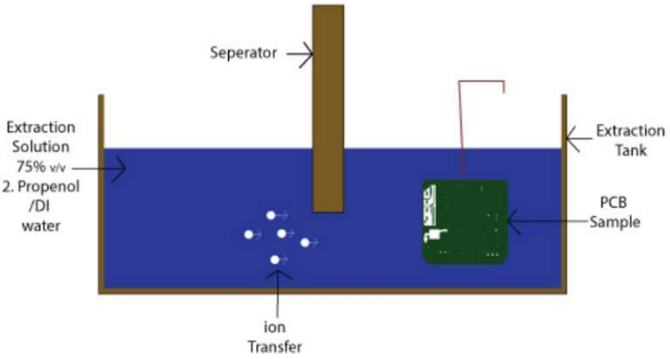
5.0 Cleaniness Testing

Mesure de la contamination ionique (avant Solder mask)
Selon IPC TM 650 method 2.3.25.1 « Ionic Cleanliness Testing of Bare PWBs"
§ 4 Apparatus: Resistivity of Solvent extract (ROSE)



A réaliser avant dépôt de solder mask !

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5.0 Cleaniness Testing

LIMITS

Type	Limit
Bare Board (PCB nu) fin de process	**0,75 ug eq NaCL/cm²**
PCBA (PCB equipé) Avant conf coat	**1,56 ug eq NaCL/cm²**

Malaise !!
https://www.eptac.com/faqs/ask-helena-leo/ask/ipc-5704-vs-ipc-6012-bare-board-cleanliness-comparison

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5.0 Cleaniness Testing

Countermeasure at PCB manufacturer as well as at PCBA manufacturer

1. Work stations should be kept clean and neat.
2. There should be no eating, drinking or use of tobacco products at the work station or other activities that are likely to cause contamination of the board surfaces.
3. Hand creams and lotions containing silicone should not be used since they could result in solderability and other processing problems. Specially formulated lotions are available.
4. Handling of boards by their edges is desirable.
5. Lint free cotton or disposable plastic gloves should be used when handling bare boards. Gloves should be changed frequently as dirty gloves can cause contamination problems.
6. Unless special racks are provided, stacking boards without interleaving protection should be avoided.

At a minimum, PCB manufacturers should clean the PCB:

- Immediately before the application of solder resist
- Immediately after the application of any solderability plating

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5.0 Cleaniness Testing

Impact of ionic contamination on PCB and PCBA ➔ See Module A-3.1 Trouble shooting on PCBA

9. Corrosion and ECM and CAF On PCBA

Countermeasures :

- ❑ Low halogen for solder paste (ROL0) or cleaned PCBA
- ❑ Fine tuning on profile management (Soak)
- ❑ Flux just the minimum at solder wave
- ❑ Gloves or finger tip wearing
- ❑ Conformal coating
- ❑ Measure regularly ionic contamination (IPC TM 650 2.3.25)

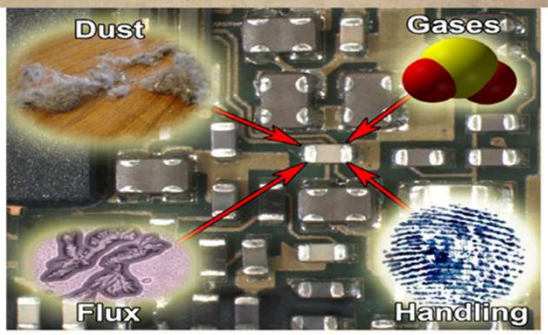

Figure 1.7: Illustration of some common contaminants that could influence corrosion properties of electronics.

Many ionic contaminants are also often hygroscopic and help forming a condensed water layer at lower humidity levels.

52

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5.0 Cleaniness Testing

Impact of ionic contamination on PCB and PCBA ➔ See Module A-3.1 Trouble shooting on PCBA

ECM : Electro Chemical Migration

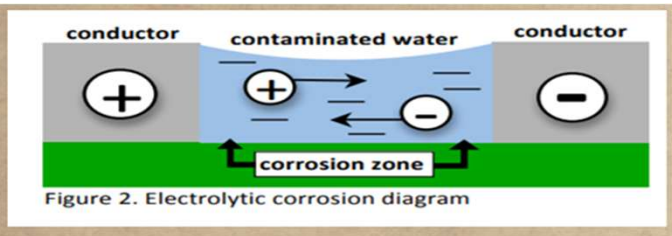

Figure 2. Electrolytic corrosion diagram

Countermeasures :

- Low halogen for solder paste (ROL0) , or cleaned PCBA
- Fine tuning on profile management (Soak)
- Flux just the minimum at solder wave
- Caution on solder pallet (selective)
- Gloves or finger tip wearing
- Measure regularly ionic contamination

53

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5.0 Cleaniness Testing

Impact of ionic contamination on PCB and PCBA ➔ See Module A-3.1 Trouble shooting on PCBA

ECM : Electro Chemical Migration

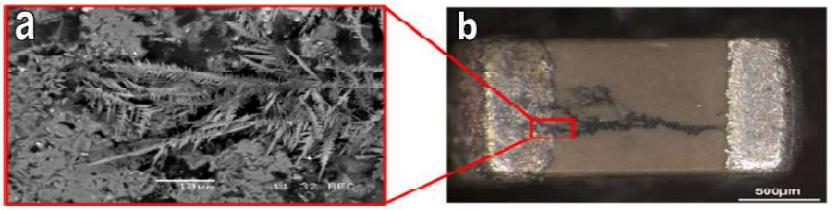


Figure 3.3: Example of electrochemical migration on a ceramic chip resistor: a) SEM image of the dendrite-anode contact point and b) optical microscopy image showing the whole dendrite. The cathode is on the right and the anode is on the left.

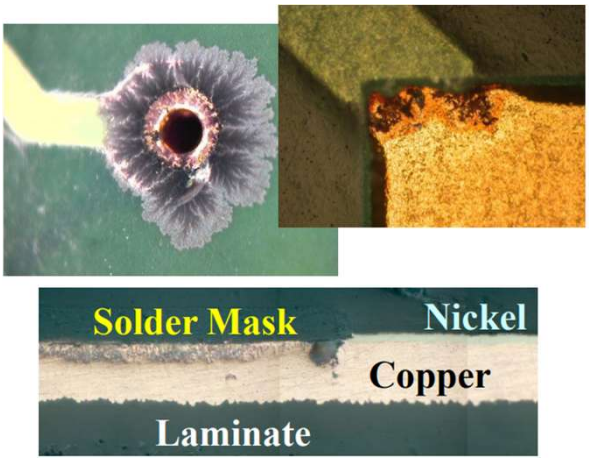
54

54

5.0 Cleaniness Testing

Impact of ionic contamination on PCB and PCBA ➔ See Module A-3.1 Trouble shooting on PCBA

Corrosion



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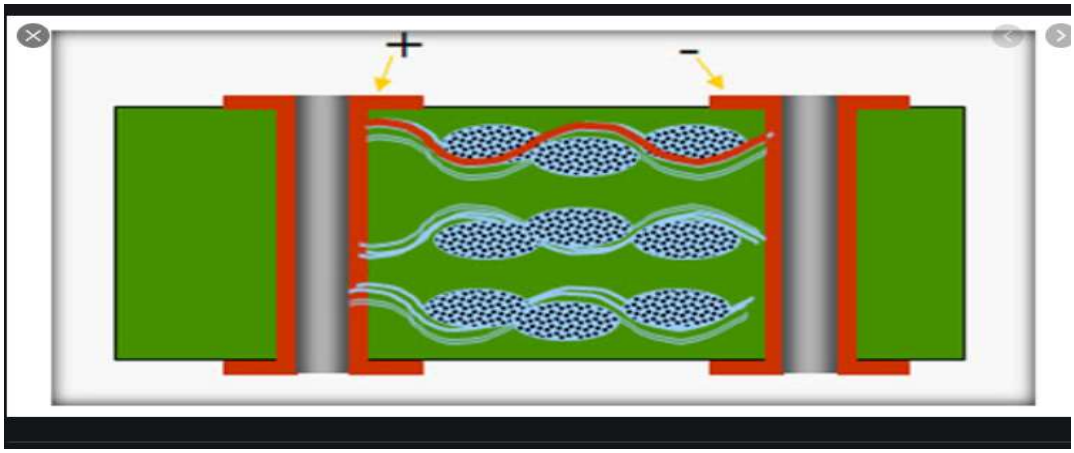
55

5.0 Cleaniness Testing

Impact of ionic contamination on PCB and PCBA ➔ See Module A-3.1 Trouble shooting on PCBA

CAF : Conductive anodic Filament



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5: l'IPC 9121 : Troubleshooting for Printed Board Fabrication processes

6.1.2 Hole Quality

Issue: Excessive resin smear

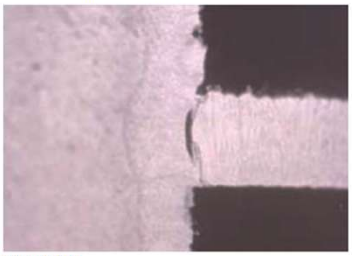

Figure 6.1.2-1

CAUSE	ACTION
Improper feeds/speeds	Optimize feed/speed relationship
Excessive dwell time in hole	Change feed/speed relationship to reduce dwell time (change chip load) Reduce stack height Check drill bit sharpness Drill pilot holes before drilling final hole size Check stroke dwell (bottom) Check RPM fall-off
Material not fully cured	Bake material before drilling
Excessive number of hits	Limit number of hits per drill bit
Drill bits resharpened too many times or past acceptable flute length	Limit number of times drill bit can be resharpened (a common limit is total drill length)
Backup and entry material	Change material

57

57

5: l'IPC 9121 : Troubleshooting for Printed Board Fabrication processes

Issue: Conductive anodic filament (CAF)

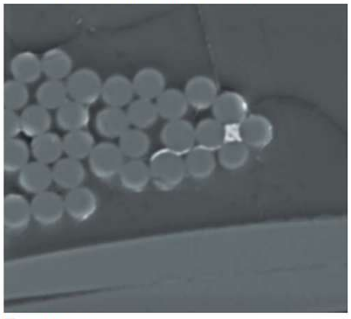

Figure 11.4.1-1

CAUSE	ACTION
Laminate moisture content	Bake-out of laminate
Weak glass-to-resin bond strength	Confirm manufacturer's recommended storage parameters
High levels of ionic impurities	Use anti-CAF treatment Improve rinsing process
Poor hole wall quality	Sharpen or replace drill bits Calibrate drill machine

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FRAMATECH

CYCLE : Performance électronique

LES EXIGENCES DE L'IPC A 600

Partie C

Les trouble shooting

FRAMATECH S.A. au capital de 38112 Euros
Etudes & mises en œuvre de stratégies industrielles internationales Hautes Technologies

4 boulevard d'Arras - 13004 Marseille - France
Tél. +33 491 95 55 70 | Mail : contact@framatech.fr
Organisme de formation n° 93060115506 | Siret 344 351 879 00046 | NAF 742C
Web : www.framatech.fr

Partie C : Les Trouble Shooting

1 : Delamination

2: Soudabilité : démouillage, non mouillage, black pad

3 : CAF

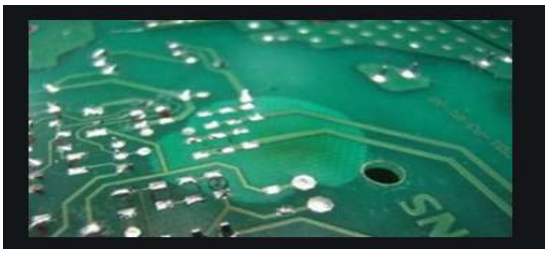
4: Exemples de DFM pour limiter les trouble Shooting

5 : Beaucoup d'autres trouble shooting sont décrits dans l'IPC 9121 : ***Troubleshooting for Printed Board Fabrication processes***

1

1

1 : Delamination



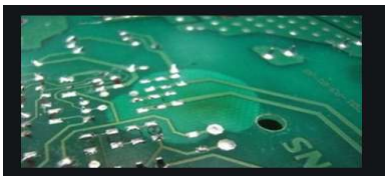
Red X factors :

- ❑ Bonding issue during PCB lamination (see module A4,1 PCB construction)
- ❑ Moisture absorption (baking should have been performed)

2

2

1 : Delamination



Moisture absorption countermeasures

1) **Prevent moisture absorption (MBB (moisture Barrier bag) / Dry pack)**
2) **Backing**

Backing of PCB recommendations on IPC 1601
« Printed Board handling and storage guidline »

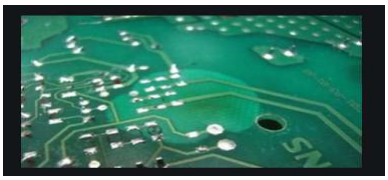
Table 3-1 Recommendations for Printed Board Baking Profiles

Final Finish	Temperature	Time	Comments
Tin	105 – 125 °C	4-6 Hours	Baking may reduce solderability. See 3.4.1.5
Silver	105 – 125 °C	4-6 Hours	Silver may tarnish. See 3.4.1.4
Nickel/Gold	105 – 125 °C	4-6 Hours	See 3.4.1.2
ENEPIG	105 – 125 °C	4-6 Hours	
Organic Coating	See 3.4.1.1		
HASL/HAL	105 – 125 °C	4-6 Hours	Final surface thickness below 0.77 µm [30.0 µin] may turn into pure intermetallics and render the printed board unsolderable

3

3

1 : Delamination



Moisture absorption countermeasures

1) **Backing**

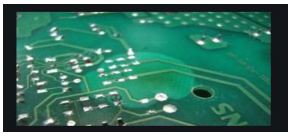
Backing should be minimized
If Performed, follow the backing rules and use an appropriated oven
(dry air if possible, good airflow, separation between PCB …)

Storage can be performed under dry air cabinet, or under dry pack

4

4

1 : Delamination



IPC 1601

Zvei documentation on this IPC 1601 Standard :
https://www.zvei.org/fileadmin/user_upload/Verband/Fachverbaende/PCB_and_Electronic_Systems/Schlau_entwickelt_clever_produziert._Leiterplatten_aus_Europa/pdf/Engl_2021/ZVEI_Recommendations_to_IPC_1601_2021_06.pdf

Countermeasures :
See IPC 1601 (§ 3.3.6 , or Zvei recommendations)

3.3.6 **Recommended Moisture Levels Prior to Packaging**
To ensure that printed boards are sufficiently dry when they are ready to solder, both the printed board fabricator and the user should protect them from moisture uptake.
Both parties should implement effective process controls and protective packaging to limit the exposure of printed boards to ambient humidity during processing and storage.

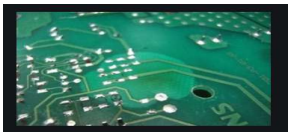
5

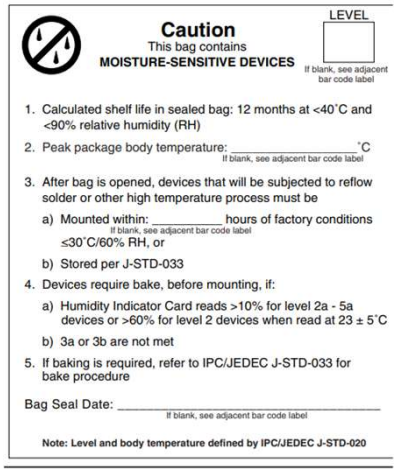
5

1 : Delamination

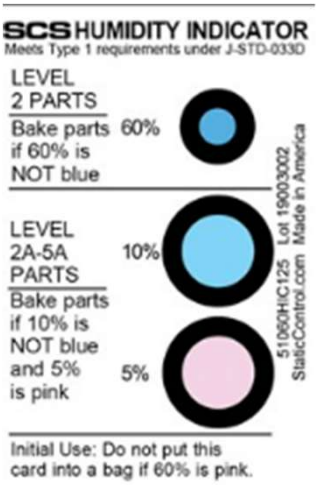
Moisture preservation ➔ IPC/JSTD 033

MSL : Moisture sensitive Level





Labelling with MSL Level



HIC Humidity Indicator Card

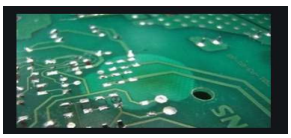
Dessicant

6

6

1 : Delamination

Moisture preservation ➔ IPC/JSTD 033



PCB packing can be with aluminium bag (Dry Pack), or under blister.

7

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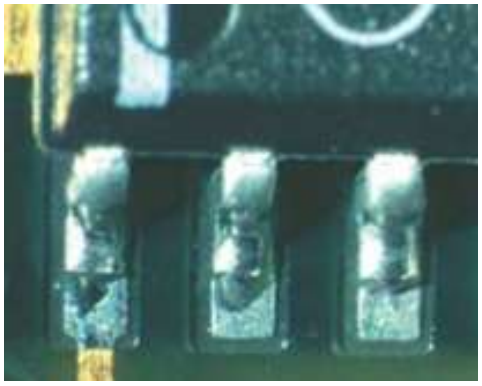
2 : Soudabilité

Démouillage :



De wetting at PCB land side

Root cause 1 :

1) Oxydation (storage condition)
Oxygen and moisture
MBB(dry pack) is a good countermeasure

Occures on HASL, ImTin, OSP, ENIG

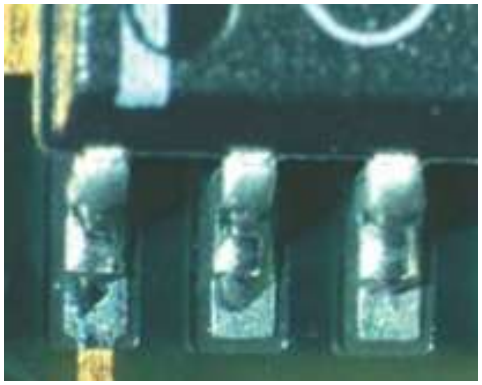
Possibility to remove oxydes with acid
(very special process !!)

8

8

2 : Soudabilité

Démouillage :



De wetting at PCB land side

Root cause 2:

2) Black PAD

9

9

Black Pad On ENIG process

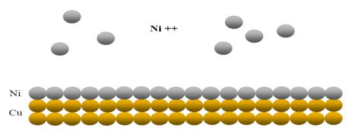


Figure 2.1: Electroless Nickel Plating

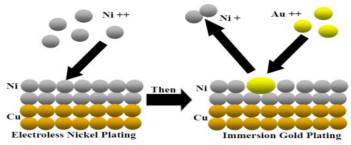


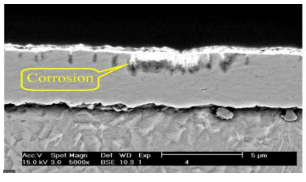
Figure 2.2: Electroless Nickel / Immersion Gold Plating

Ni Thickness : 5 µ
Au Thickness : 50 nm
IPC 4552

Immersion gold on Nikel plating is a violent oxydo reduction reaction (substitution)

Phosporus in Nikel to quiet the reaction
Not enough P ➔ Nikel too oxidized ➔ Black Pad (hyper oxidation/Corrosion)
Too much P ➔ Sn will not come in substituion to build IMC

6 % < P < 14 %



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Black Pad On ENIG process

No solder visible on the pad (all on the cpt side)
The pad surface appeared « black » and clean

The root cause is the % of Phosporus in the Nickel
Too few ➔ oxydation of the Nickel beneath the gold
Too much ➔ the phosporous atoms prevent the diffusion of the Sn atoms

Should be between 6 and 14 %

ENIG plating is not so trivial ! .
Must be controled
Less and less issue than in the past with major suppliers

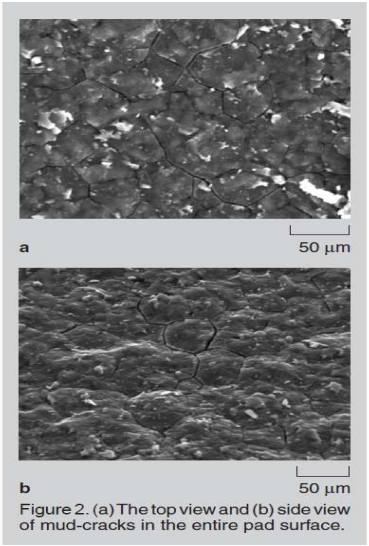

Figure 2. (a) The top view and (b) side view of mud-cracks in the entire pad surface.

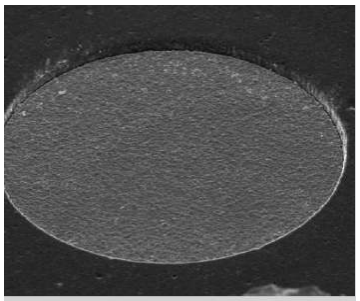
Figure 1. A 30-degree tilt view of a black pad. The pad surface appeared clean. Only a small amount of fine IMC particles (gray) and little solder residue were present on the pad.

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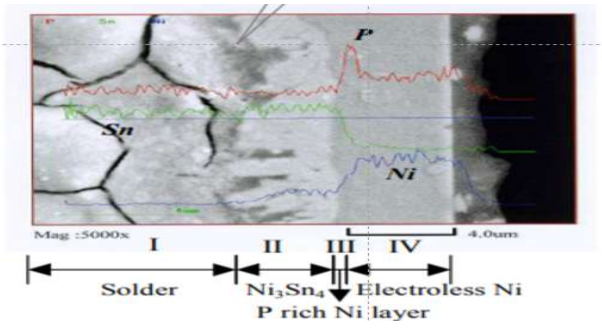
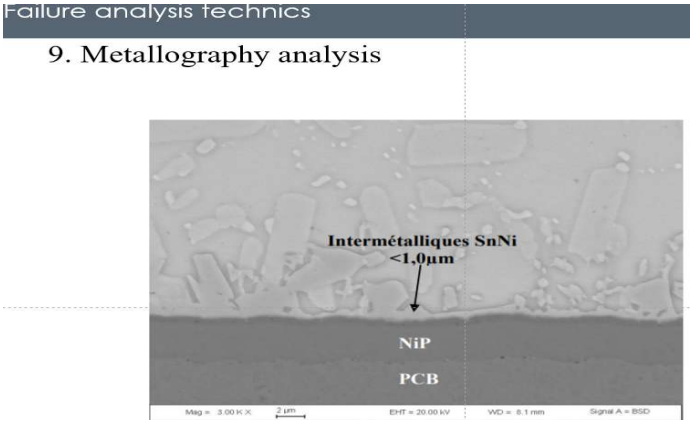
Black Pad On ENIG process





Immersion gold is a violent oxydo reduction reaction

12

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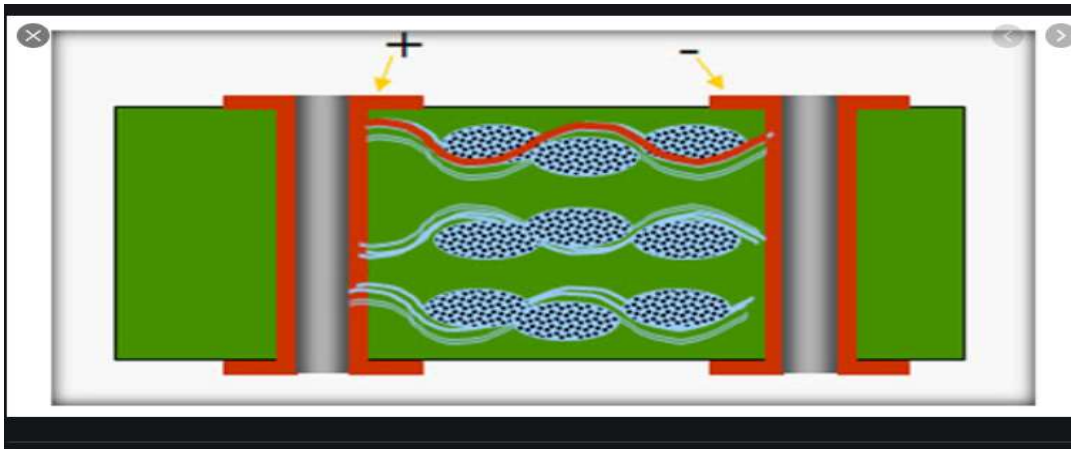
3 : CAF (Conductive Anodic Filament)



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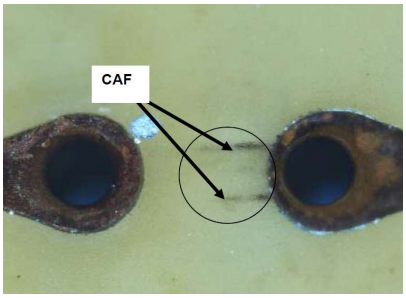
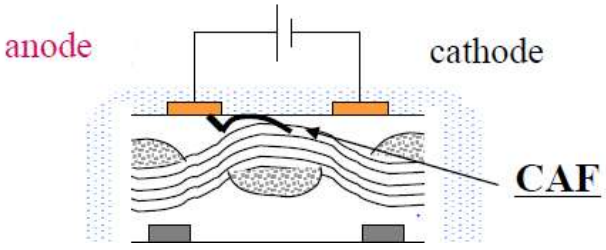
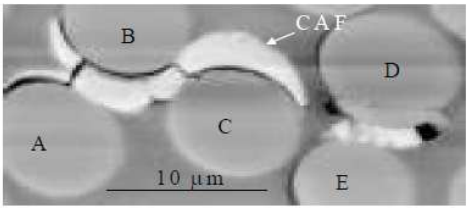
3 : CAF (Conductive Anodic Filament)

Le phénomène CAF est un processus électrochimique qui entraîne une migration d'ions cuivre de l'anode vers la cathode, entre la résine et les fibres de verre

+ -







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3 : CAF (Conductive Anodic Filament)

CAF Countermeasures

1) Anti CAF pre preg and Laminate (to be specify in PCB specification)

2) Ionic cleaniness and moisture protection at PCB Manufacturer

Cf / IPC 1601
§3.1.1 « RINTED BOARD FABRICATION AND PACKAGING (HANDLING)"

- Handle prepreg by the edges using clean latex or nitrile gloves
- Store prepreg flat in a cool, dry environment (< 23 °C [73 °F], < 50% RH)
- Reseal opened bags of unused prepreg

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4: Exemples de DFM pour limiter les trouble Shooting

Definition

Methodologie pour évaluer et anticiper les problemes dans le cycle de vie du produit (mais essentiellement en fabrication) au delà des fonctions principales du produit concu.

Fonctions de base :
FFFC (Fit, Form, Function, coût,…)

Autres fonctions (contraintes) :
Fabricabilité, testabilité, fiabilité, sourcing….

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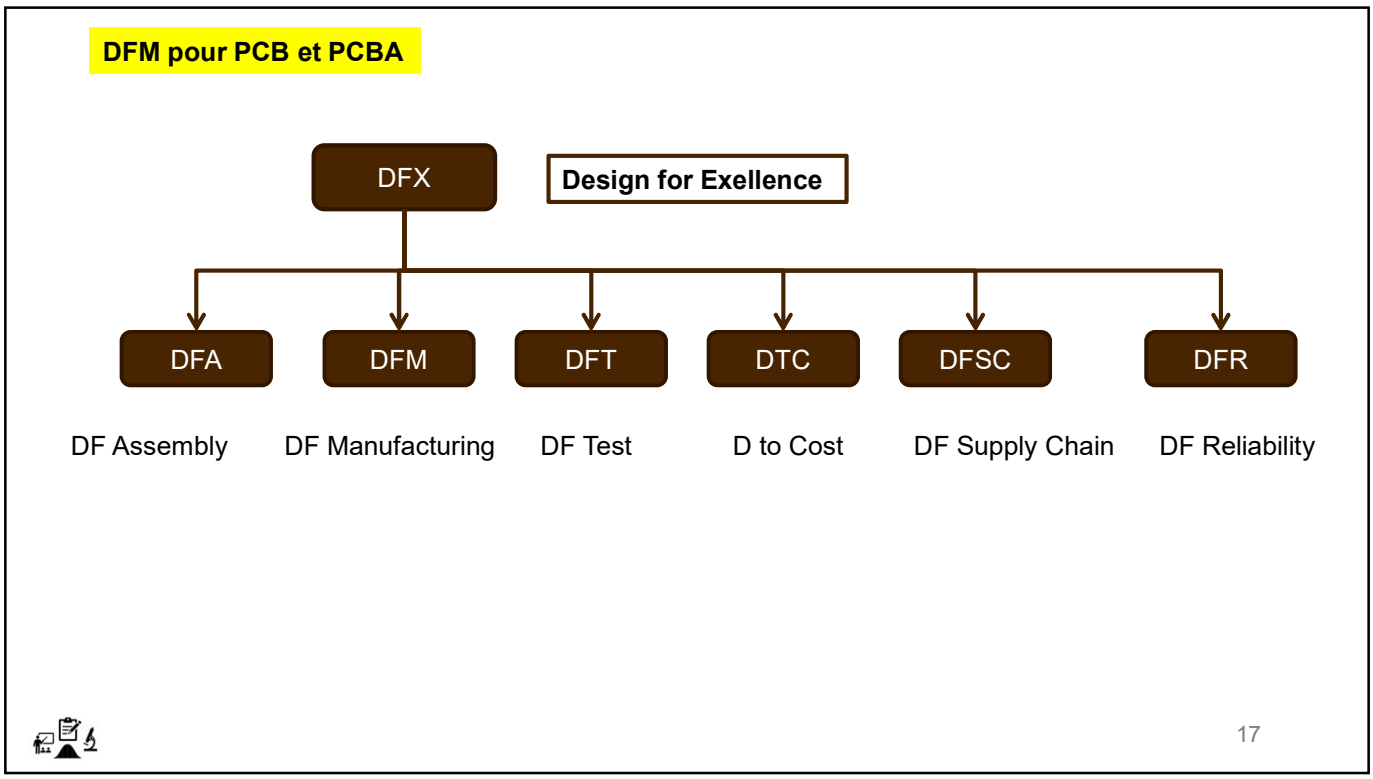
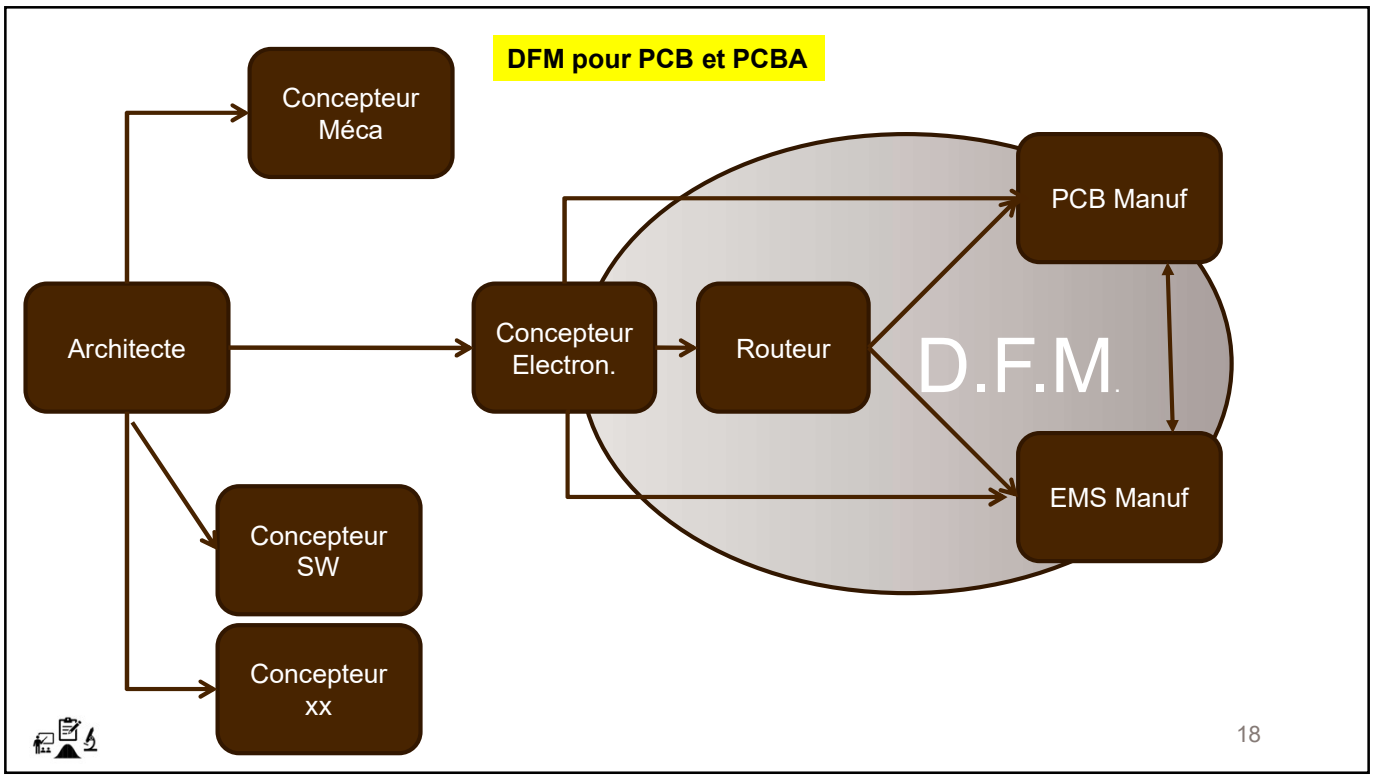

DFM pour PCB et PCBA
DFX
Design for Exellence
DFA
DFM
DFT
DTC
DFSC
DFR
DF Assembly
DF Manufacturing
DF Test
D to Cost
DF Supply Chain
DF Reliability
17

17


DFM pour PCB et PCBA
Concepteur Méca
Architecte
Concepteur Electron.
Routeur
PCB Manuf
D.F.M.
EMS Manuf
Concepteur SW
Concepteur xx
18

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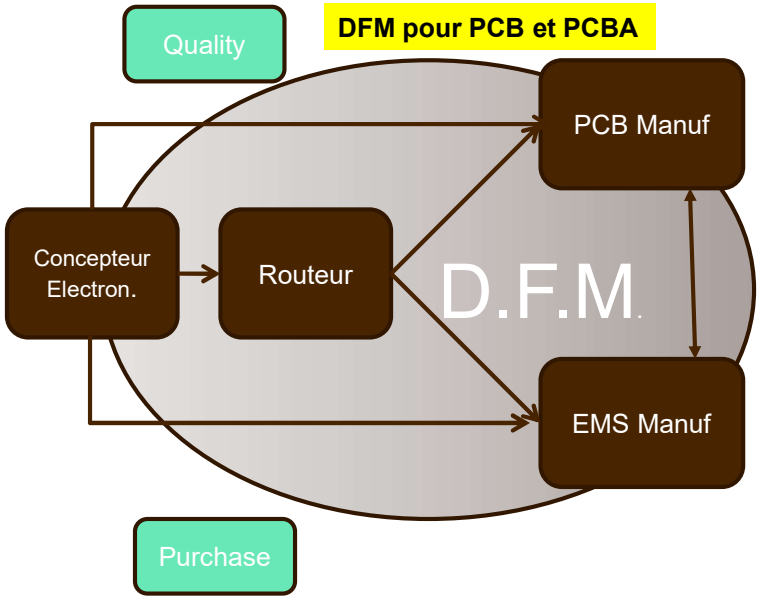
DFM pour PCB et PCBA



- **Toutes ces parties prenantes sont expertes dans leur domaine.**
- **Elles doivent se « parler » continuement.**
- **Le vocabulaire et la grammaire de cette communication se trouvent dans les IPC.**
- **Chacun doit connaitre les grandes lignes des contraintes des autres partie prenantes**
- **La communication est basée sur la confiance et l'open book**

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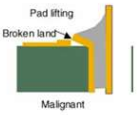
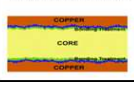
DFM pour PCB et PCBA

On part des évenements redoutés, dont on a le florilège dans le module « Les Trouble Shooting en PCBA «

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
1	Important Stress during reflow		Tg	Require High Tg		170 ° C
2	Pad lifting		CTEz	Low CTEz aftre Tg		< 300 PPM
			Tg	High Tg		170 ° C
			Cu Tooth profile	Std or Lox profile Not very low		See IPC 4562

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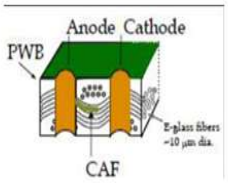
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
3	CAF		Resin	**Anti CAF resin**		Anti Caf resin
4	PCB Bowing, Twisting, Warping		Copper filling balance	See the 4 rules slide 120		

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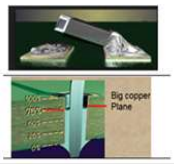
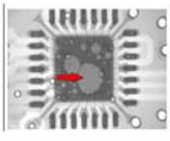
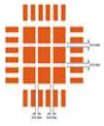
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
5	Manhattan and hole filling issue		Calories spent into big plane	Thermal relief		CAO tools (Altium, Cadence)
6	Solder voids (aminly QFN)		Gaz vapor from solder paste during reflow	Square the GND foot print		

22

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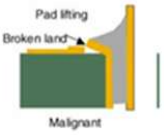
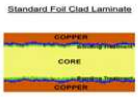
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
7	Open Circuit in internal Layer between track and Hole	 Drill Breakout	Drilling/ desmearing/ plating process	Tear Drop design	 Drill Breakout With Teardrop	
8	Pad Lifting	 	CTEz	Low CTEz after Tg		< 300 PPM
			Tg	High Tg		170 ° C
			Cu Tooth profile	Std or Low profile Not very low		See IPC 4562

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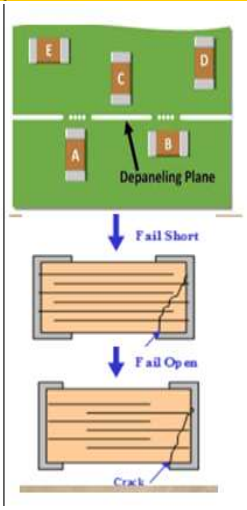
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
9	MLCC cracked capa		PCBA Bending	1) Keep out distance from border 2) Direction vs constraint 3) 2 capa in serie 4) Open Mode and/or soft term 5) Handling 6) Depanelization		

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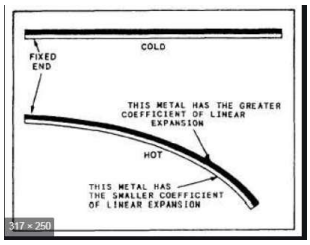
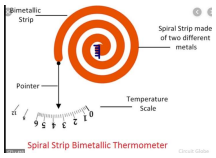
PCB Bowing/ Warping/Twisting : 4 rules for copper filling

CTE Mismatch



Benefits

PROs

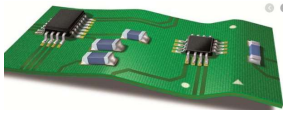


Bimetallic Effect ➔ Themometer

Drawbacks

CONs

Bimetallic Effect ➔ PCB & Cpt Warpage
(see PCB Copper Filling rules)



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1.PCB Bowing twisting warping ➔ Copper filling balance

IPC-2222

10.1.2 Balanced Conductors Whenever possible, to reduce bow and twist and to increase dimensional stability, conductors should be balanced within an individual layer. Conductor routing density should be spread throughout the board wherever possible, to avoid the need for special etching or plating thieves.

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The multilayer printed board structure should also be as balanced as possible providing equal layers of signal conductors and planes to either side of the center of the multilayer construction.

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1.PCB Bowing /twisting /warping ➔ Copper filling balance

- Rule 1 : Layer thickness in mirror (#1 with #n , #(1+1) with #n-1 ……etc)
- Rule 2 Balanced copper (etching)in mirror layers (% filling #1 = %filling # n)
- Rule 3 :Balanced copper (etching) within each layer
- Rule 4 : Total symmetry of a core (thickness, % copper filling, and pattern)

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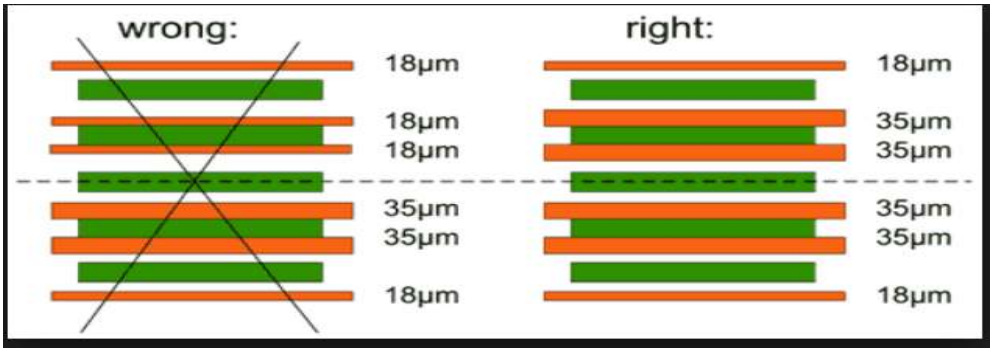
Rule 1 : Layer thickness in mirror



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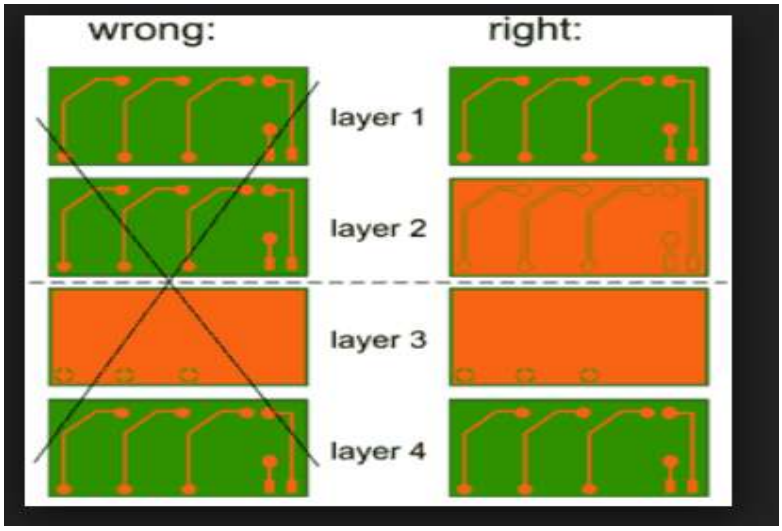
Rule 2 Balanced copper (etching)in mirror layers



18µ	10 %	layer 1	10 %
35µ	10 %	layer 2	85 %
35µ	90 %	layer 3	90 %
18µ	10 %	layer 4	10 %

29

29

Rule 3 : Balanced copper (etching) within each layer

Wrong Correct

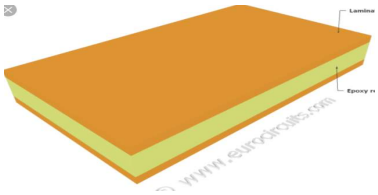
- Make sure that your panels have an even copper distribution on each layer and between different layers. If needed add extra copper patterns inside the circuits, in between the PCB"s or in the panel border.

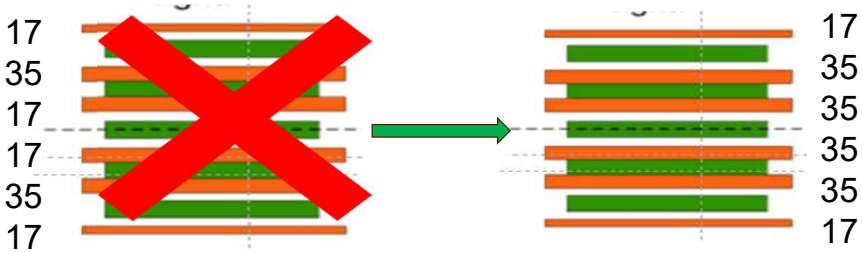
- Enhance copper distribution
- Evenly distributed copper enhances the overall quality of the panel:
  - Better mechanical stability (reduced risk for bow and twist)
  - well balanced copper plating in the PTH holes and on the copper pattern.

30

30

Rule 4 : Total symetry on a core (thickness, % copper filling, and pattern)





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Biblio

« The desginer's Handbook for DFM / Sierra Circuits

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DFM vs IPC A 600
Design For Manufacturing

1

1

D.F.M.

Definition

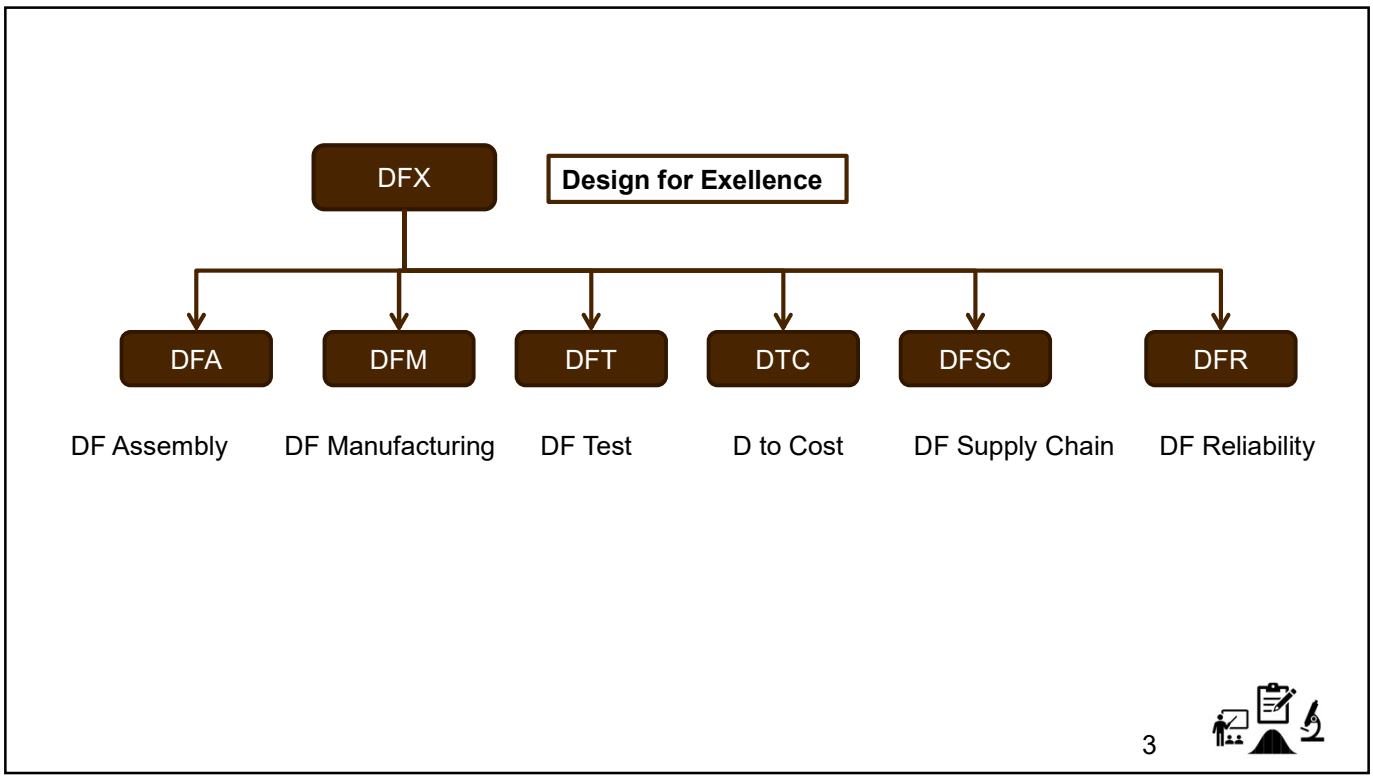
Methodologie pour évaluer et anticiper les problemes dans le cycle de vie du produit (mais essentiellement en fabrication) au delà des fonctions principales du produit concu.

Fonctions de base :
FFFC (Fit, Form, Function, coût,…)

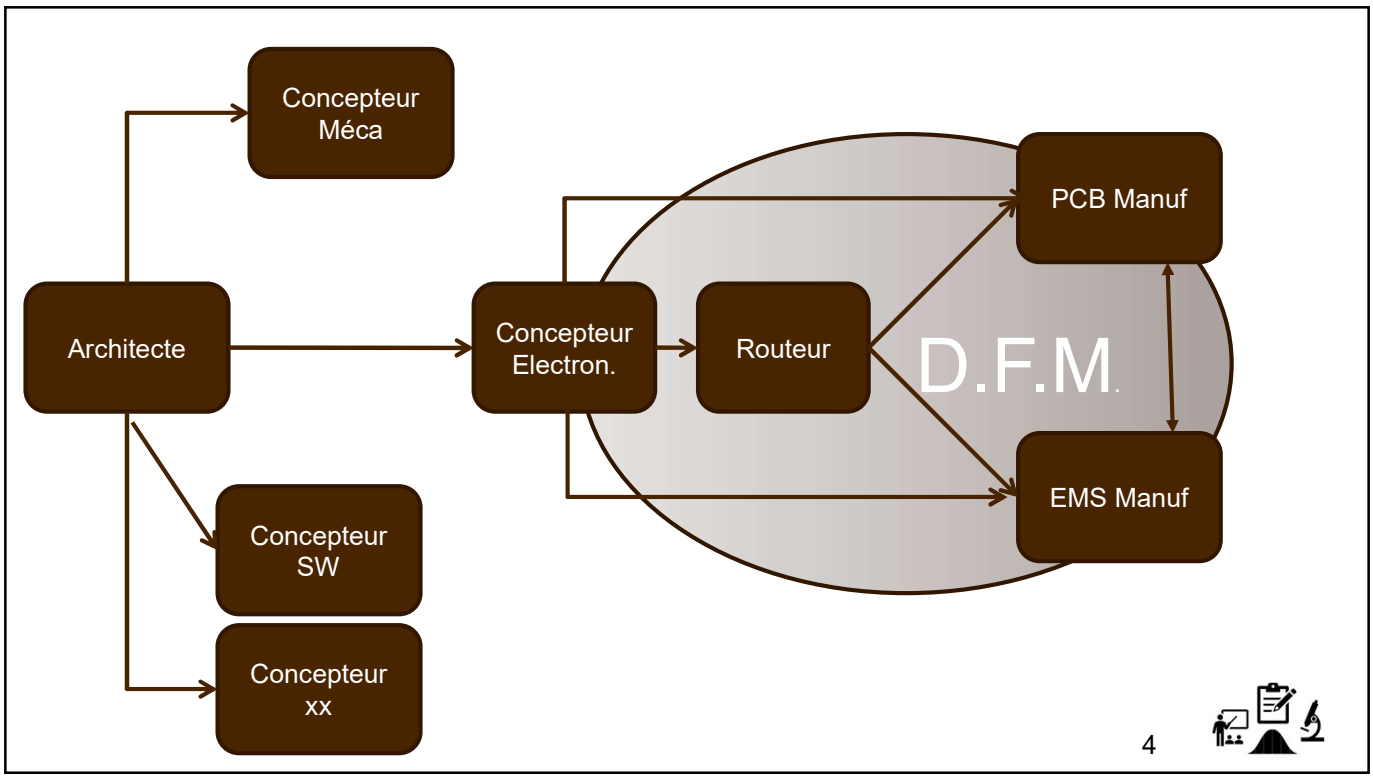
Autres fonctions (contraintes) :
Fabricabilité, testabilité, fiabilité, sourcing….

2

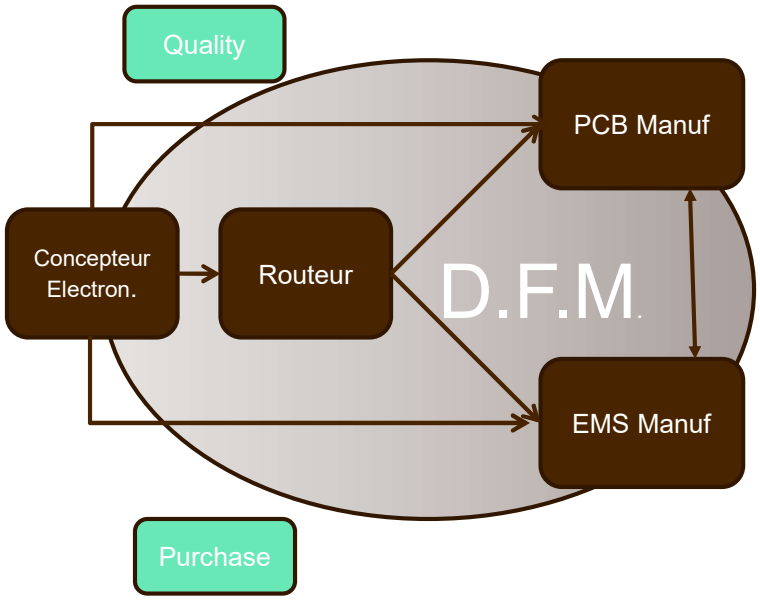
2


DFX
Design for Exellence
DFA
DFM
DFT
DTC
DFSC
DFR
DF Assembly
DF Manufacturing
DF Test
D to Cost
DF Supply Chain
DF Reliability
3

3


Concepteur Méca
Architecte
Concepteur Electron.
Routeur
PCB Manuf
D.F.M.
EMS Manuf
Concepteur SW
Concepteur xx
4

4



- **Toutes ces parties prenantes sont expertes dans leur domaine.**
- **Elles doivent se « parler » continuement.**
- **Le vocabulaire et la grammaire de cette communication se trouvent dans les IPC.**
- **Chacun doit connaitre les grandes lignes des contraintes des autres partie prenantes**
- **La communication est basée sur la confiance et l'open book**

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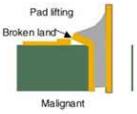
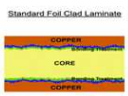
DFM pour PCB et PCBA

On part des évenements redoutés, dont on a le florilège dans le module « Les Trouble Shooting en PCBA «

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
1	Important Stress during reflow		Tg	Require High Tg		170 ° C
2	Pad lifting		CTEz	Low CTEz aftre Tg		< 300 PPM
			Tg	High Tg		170 ° C
			Cu Tooth profile	Std or Lox profile Not very low		See IPC 4562

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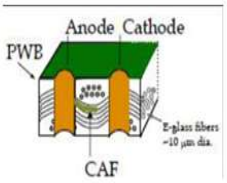
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
3	CAF		Resin	**Anti CAF resin**		Anti Caf resin
4	PCB Bowing, Twisting, Warping		Copper filling balance	See the 4 rules slide 120		

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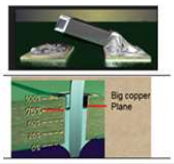
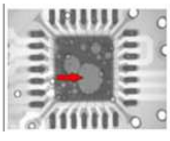
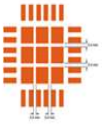
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
5	Manhattan and hole filling issue		Calories spent into big plane	Thermal relief		CAO tools (Altium, Cadence)
6	Solder voids (aminly QFN)		Gaz vapor from solder paste during reflow	Square the GND foot print		

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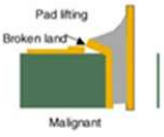
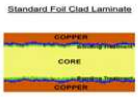
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
7	Open Circuit in internal Layer between track and Hole	 Drill Breakout	Drilling/ desmearing/ plating process	Tear Drop design	 Drill Breakout With Teardrop	
8	Pad Lifting	 	CTEz	Low CTEz after Tg		< 300 PPM
			Tg	High Tg		170 ° C
			Cu Tooth profile	Std or Low profile Not very low		See IPC 4562

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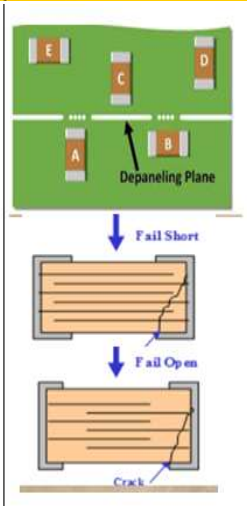
DFM pour PCB et PCBA

Item	Feared event	Picture	Factor	Countermeasure / Rule	Picture	Specification
9	MLCC cracked capa		PCBA Bending	1) Keep out distance from border 2) Direction vs constraint 3) 2 capa in serie 4) Open Mode and/or soft term 5) Handling 6) Depanelization		

10

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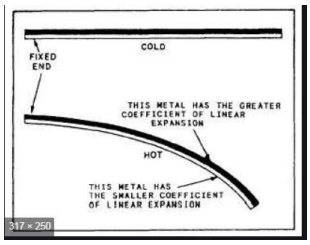
PCB Bowing/ Warping/Twisting : 4 rules for copper filling

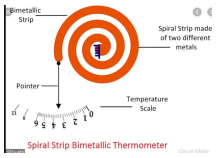
CTE Mismatch



Benefits

PROs

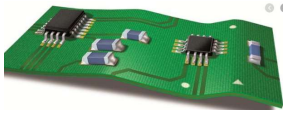
Bimetallic Effect ➔ Themometer



Drawbacks

CONs

1) Bimetallic Effect ➔ PCB & Cpt Warpage
(see PCB Copper Filling)



2) Solder cracks

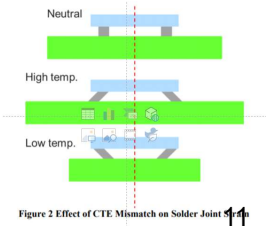


Figure 2 Effect of CTE Mismatch on Solder Joint Strain

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1.PCB Bowing twisting warping ➔ Copper filling balance

IPC-2222

10.1.2 Balanced Conductors Whenever possible, to reduce bow and twist and to increase dimensional stability, conductors should be balanced within an individual layer. Conductor routing density should be spread throughout the board wherever possible, to avoid the need for special etching or plating thieves.

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12

12

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- Rule 4 : Total symmetry of a core (thickness, % copper filling, and pattern)

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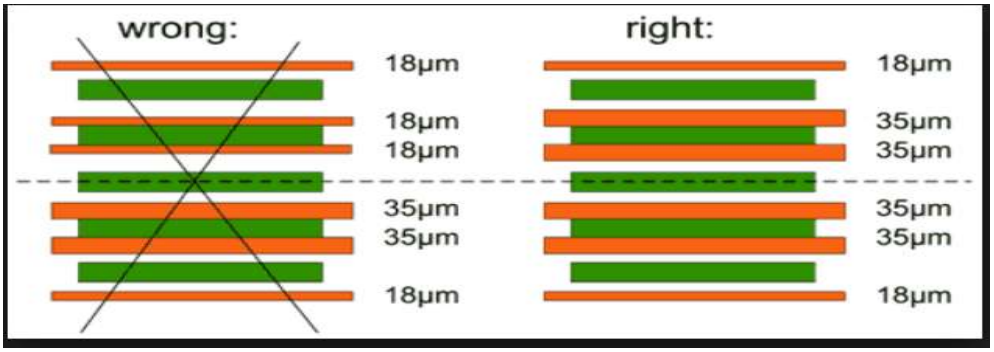
Rule 1 : Layer thickness (oz) in mirror



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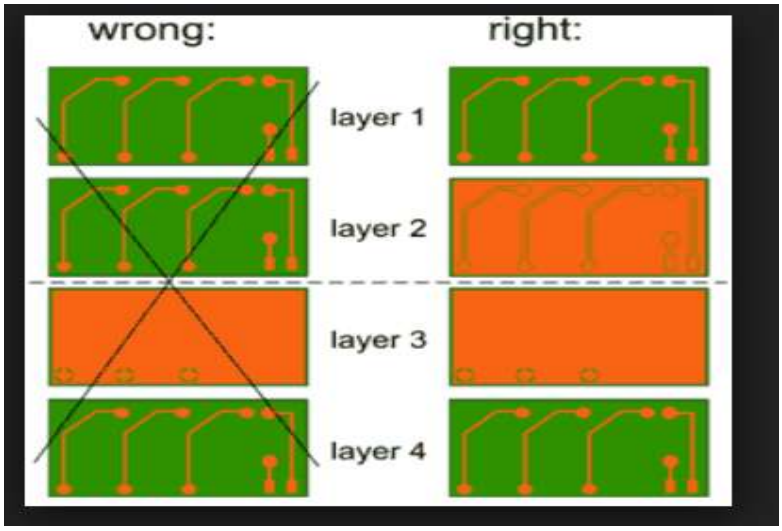
Rule 2 Balanced copper (etching)in mirror layers



18µ	10 %	layer 1	10 %
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15

15

Rule 3 : Balanced copper (etching) within each layer

Wrong Correct

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- Enhance copper distribution
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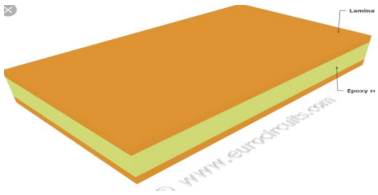
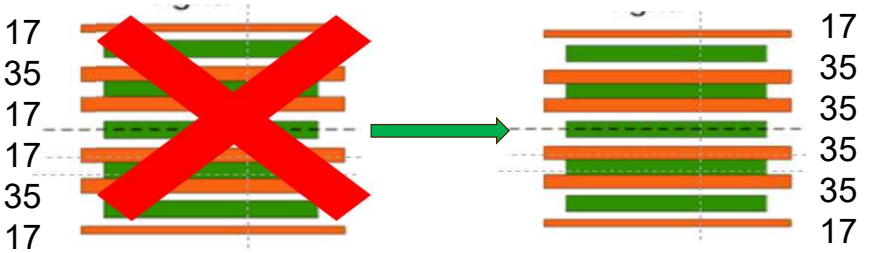
Rule 4 : Total symetry on a core (thickness, % copper filling, and pattern)





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Biblio

« The desginer's Handbook for DFM / Sierra Circuits

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FRAMATECH

CYCLE : Performance électronique

LES EXIGENCES DE L'IPC A 600

Partie D

Documentation accompagnant la livraison (rapports de test/ CofC/ FAI)

FRAMATECH S.A. au capital de 38112 Euros
Etudes & mises en œuvre de stratégies industrielles internationales Hautes Technologies

4 boulevard d'Arras - 13004 Marseille - France
Tél. +33 491 95 55 70 | Mail : contact@framatech.fr
Organisme de formation n° 93060115506 | Siret 344 351 879 00046 | NAF 742C
Web : www.framatech.fr

Partie D : Documentation accompagnant la livraison (rapports de test/ CofC/ FAI..)

1

1

Documentation accompagnant la livraison

ITEM	DESCRIPTION		TEST METHOD	NO. OF SAMPLE	SPEC	RESULTS	REMARKS
1	LAMINATE MATERIAL		NA	NA	FR-4	FR-4	
2	BOARD THICKNESS		IPC-6012C 3.4	5 ARRAY	0.0647"±0.0064"	0.0637 "	
3	FLAMMABILITY CLASS		IPC-6012C 3.2.1	NA	94V-0	94V-0	
4	CONDUCTOR WIDTH		IPC-6012C 3.5.1	5 ARRAY	0.00360"~0.00492"	0.0048 "	
5	CONDUCTOR SPACE		IPC-6012C 3.5.2	5 ARRAY	0.00320"~0.00480"	0.0040 "	
6	ANNULAR RING		IPC-6012C 3.4.2	5 ARRAY	MIN. 0.0020"	0.0040 "	
7	CORE	THICKNESS OF CORE	IPC-6012C 3.6.2	NA	0.008"±0.001" 0.015"±0.0015"	0.00787 " 0.01468 "	
		COPPER FOIL	IPC-6012C 3.6.2	NA	follow stack up 1/1oz	1/1oz	

2

2

Documentation accompagnant la livraison

ITEM	DESCRIPTION		TEST METHOD	NO. OF SAMPLE	SPEC	RESULTS	REMARKS
8	COPPER THICKNESS	PTH	IPC-6012C 3.6.2.11	1 ARRAY	MIN. 0.0007"	0.00110 "	
		BVH			NA	NA	
		IVH			NA	NA	
		Vias filling	IPC-6012C 3.6.2.16	1 ARRAY	NA	NA	
9	S · M · MATERIAL / COLOR		IPC-6012C 3.7	NA	L.F. / GREEN	OK	
10	LEGEND MATERIAL / COLOR		IPC-6012C 3.2.10	NA	NA	NA	
11	THERMAL STRESS TEST	SURFACE	IPC-TM-650 2.6.8	1 ARRAY	288±5 C 10 SECS	OK	
		PTH			288±5 C 10 SECS	OK	
12	SOLDERABILITY TEST		ANSI/J-STD-003 test C	1 ARRAY	MIN 95%	OK	
13	ELECTRIC TEST		IPC-TM-650 2.5	ALL	• ≧250V ≦25Ω ≧30MΩ	OK	
14	Adhesion	Finich	IPC-6012C 3.7.2	1 ARRAY	NO PEELING	OK	
		Soider resist			NO PEELING	OK	

3

3

Documentation accompagnant la livraison

ITEM	DESCRIPTION		TEST METHOD	NO. OF SAMPLE	SPEC	RESULTS	REMARKS
15	TAPE TEST OF LEGEND		IPC-TM-650 2.4.1.1	1 ARRAY	NA	NA	
16	TAPE TEST OF GOLD FINGER		IPC-TM-650 2.4.1	1 ARRAY	NO PEELING	OK	
17	TAPE TEST OF SOLDER MASK		IPC-TM-650 2.4.28.1	1 ARRAY	NO PEELING	OK	
18	WARP & TWIST		IPC-TM-650 2.4.22	5 ARRAY	MAX . 0. 7%	OK	
19	SOLDER THICKNESS		IPC-6012C 3.2.7	5 ARRAY	NA	NA	
20	SOLDER MASK THICKNESS		IPC-6012C 3.7.3	5 ARRAY	0.0004"~0.0012"	0.00082 "	
21	GOLD THICKNESS		IPC-6012C 3.2.7	5 ARRAY	MIN. 1.9685μ"	2.79 μ"	
22	NICKEL THICKNESS		IPC-6012C 3.2.7	5 ARRAY	118.11-236.22μ"	221.6 μ"	
23	INOIC CONTAMINATION	BEFORE SM	BELLCORE GR-78-CORE 14.5	1 PNL	≦3.2ug NaCl / sq.in	0.37ugNaCl / sq.in	
		AFTER FINISH		1 ARRAY	≦3.2ug NaCl / sq.in	0.00ugNaCl / sq.in	

4

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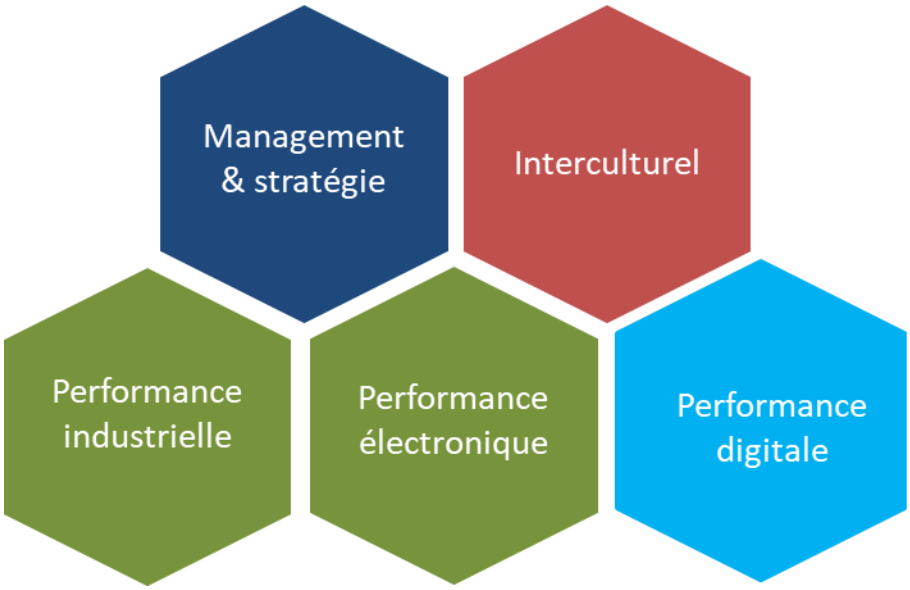
FRAMATECH

Une offre de formations adaptée à vos situations professionnelles



Contact

Alain BARONI – Président, Directeur Général
Tél. 04 91 95 55 70
Mail : contact@framatech.fr